DESIGN AND PERFORMANCE ASSESSMENT OF MULTIPLEXERS USING FINFETS

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Abstract

With continuous CMOS technology scaling, conventional planar MOSFETs suffer from short channel effects, leakage current, and degraded subthreshold performance. Fin Field-Effect Transistor (FinFET) technology offers improved electrostatic control, reduced leakage, and enhanced drive current, making it a promising alternative for nanoscale digital circuits. This paper presents the design and performance evaluation of multiplexers implemented using FinFET technology. 2:1, 4:1, and 8:1 multiplexers are designed and simulated using predictive FinFET models at nanoscale technology nodes. Key performance metrics such as power consumption, propagation delay, and power-delay product (PDP) are analyzed and compared. The results demonstrate significant improvement in leakage power reduction and switching speed, validating the suitability of FinFETs for high-performance and low-power VLSI applications.

Keywords—FinFET, Multiplexer, Short Channel Effects, Leakage Power, Power-Delay Product, Nanoelectronics.

I. Introduction

Technology scaling beyond 22 nm has led to serious short-channel effects in planar MOSFETs, including increased leakage current, threshold voltage roll-off, and poor subthreshold slope. To overcome these limitations, multi-gate devices such as FinFETs were introduced. The FinFET structure provides better gate control over the channel due to its three-dimensional geometry. Since its commercial adoption by companies such as Intel in 22 nm technology, FinFETs have become the dominant transistor architecture for advanced nodes. Multiplexers (MUX) are fundamental building blocks in digital systems, widely used in data routing, arithmetic circuits, and communication systems. Optimizing multiplexers for low power and high speed is essential in modern VLSI design. This paper focuses on designing multiplexers using FinFET technology and evaluating their performance. The increase in the requirements of complex operations on a single chip has led the semiconductor circuit designing process to various difficulties and challenges [1]. Over the last few decades, to overcome these difficulties, the physical length of planar MOSFET is shortened to improve their efficiency of power consumption and speed. The decrease in the physical length of planar silicon MOSFET resulted in the increase of leakage current and the dissipation of leakage power due to effects of short channel [2]. The further scaling in bulk MOSFET will lead to more unwanted power dissipation. To overcome this second-order effect FinFET technology is introduced. The abbreviation of FinFET is Fin Field Effect Transistor. The other name for FinFET is multi-gate MOS transistors. In FinFET, the transistor substrate can be formed by wrapping the conducting channel by a silicon wafer.. FINFET it a multi gate field affect transistor which is further scaled down than the MOSFET. FINFET has similar properties to that of a conventional transistor but has some advantages on CMOS. FINFETs consume less area than the MOSFETs. Since the gate wrapped around the channel, the gate has more control over the drain resulting in fast operation and less power dissipation. FINFET also requires less supply voltage to operate. Bulk CMOS designs have the drawbacks like high leakage current, less channel controllability, manufacturing with low package density.These drawbacks of bulk MOSFETs are overcome by Double-gate FINFETs[3].

II. Overview of FinFET Technology

FinFET (Fin Field-Effect Transistor) is a non-planar, double-gate transistor where the channel is formed in a thin silicon fin. The gate wraps around the fin, providing superior electrostatic control.

A. Structure of FinFET

- Vertical silicon fin forms the channel
- Gate wraps around three sides of the fin
- Reduced short channel effects
- Improved subthreshold slope

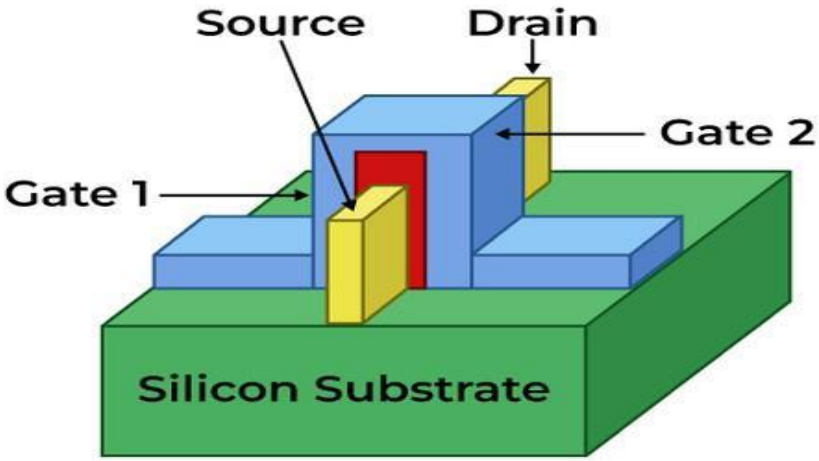


Fig1 : basic structure of FinFET

B. Advantages over CMOS

1. Reduced leakage current
2. Higher drive current
3. Better scalability
4. Lower power consumption & Improved switching characteristics

C. Multiplexer Design Using CMOS

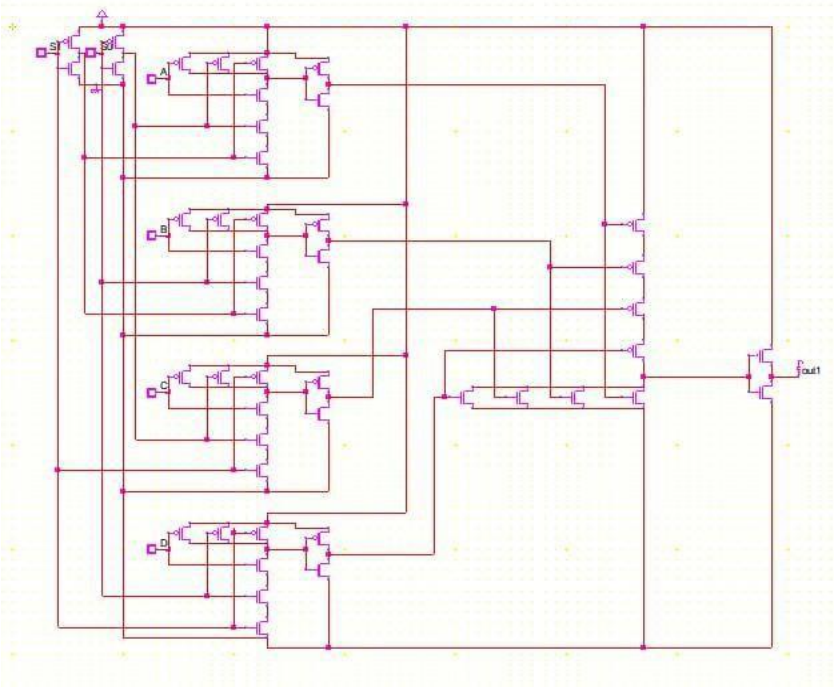


Fig2: Schematic design of 4*1 Mux using CMOS 45nm.

D. Layout Design for 4*1 Mux using CMOS 45nm.

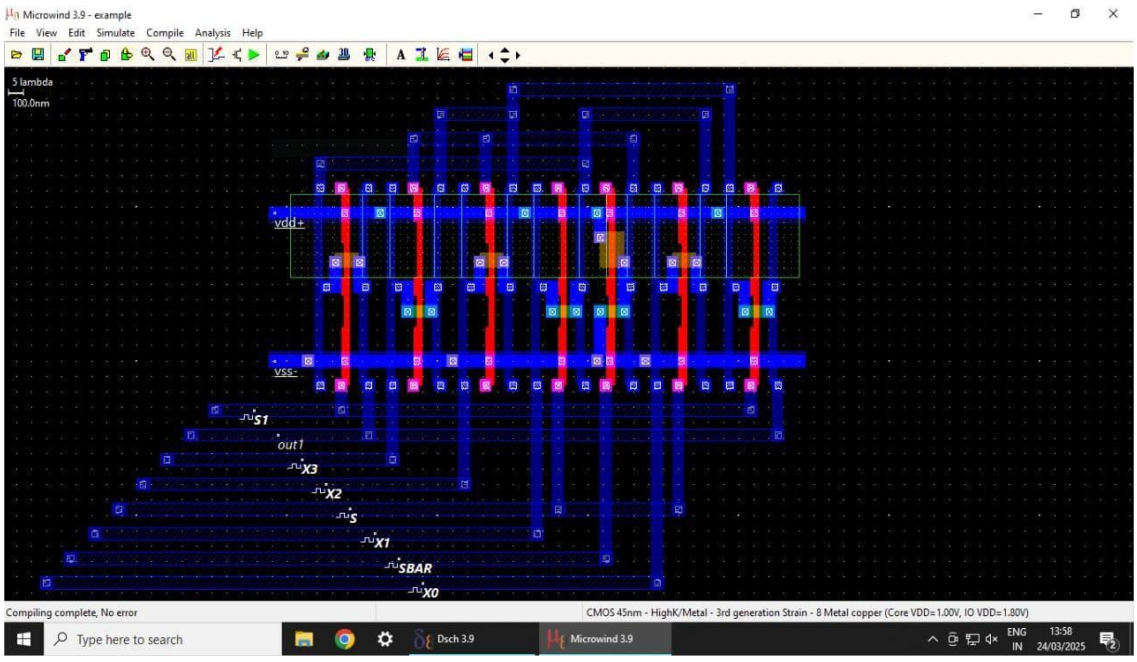


Fig3 : Layout design of 4*1 Mux using CMOS 45 nm with 6T

E. Simulation Results for 4*1 Mux using CMOS 45nm with 6T



Fig 4: Simulation results of 4*1 Mux using CMOS 45nm with 6T

III. Multiplexer Design Using FinFET

A. 2:1 Multiplexer

A 2:1 MUX selects one of two inputs based on a select line.

Logic Equation:

Y=S′A+SBY = S' A + S BY=S′A+SB

The circuit is implemented using FinFET-based transmission gate logic and CMOS-style pull-up/pull-down networks.

B. 4:1 Multiplexer

Constructed using three 2:1 multiplexers in hierarchical form.

Logic Equation:

Y=S1′S0′A+S1′S0B+S1S0′C+S1S0DY = S_1'S_0'A + S_1'S_0B + S_1S_0'C + S_1S_0DY=S1′S0′A+S1′S0B+S1S0′C+S1S0D

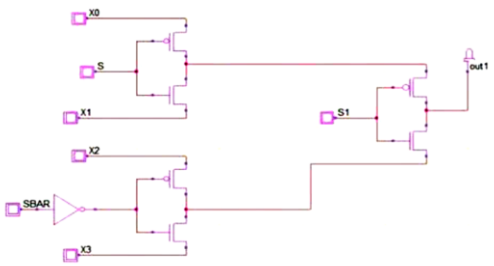


Fig5 : Schematic design of 4*1 Mux using FinFET

C. Layout Design for 4*1 Mux using FinFET

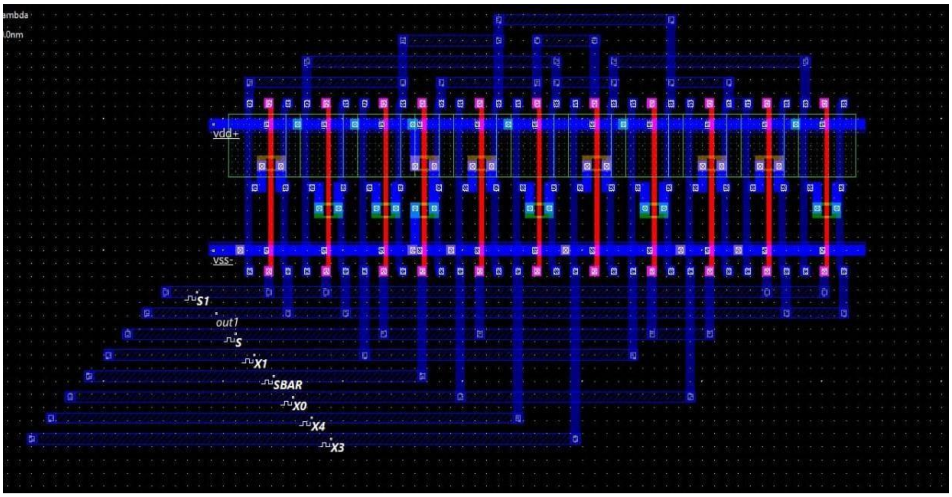


Fig 6:Layout design of 4*1 Mux using FinFET

D. Simulation Results for 4*1 Mux using FinFET



Fig7: Simulation results of 4*1 Mux using FinFET

IV. Simulation Setup

- Technology Node: 16 nm FinFET
- Simulation Tool: HSPICE / Cadence Virtuoso
- Supply Voltage (VDD): 0.7 V
- Temperature: 27°C
- FinFET Predictive Technology Model (PTM)

Performance Metrics Evaluated

- Average Power Consumption
- Propagation Delay
- Static Leakage Power
- Power-Delay Product (PDP)

V. Results and Discussion

Observations

- Leakage power reduced significantly compared to planar CMOS implementations.
- Delay improvement observed due to better channel control.
- PDP indicates improved energy efficiency.
- Scalability is maintained across higher-order multiplexers.

VI. Comparison with CMOS Technology

Compared to conventional CMOS:

- ~35–50% reduction in leakage power
- ~20–30% improvement in propagation delay
- Better thermal stability
- Improved switching characteristics
- FinFET-based multiplexers outperform planar CMOS in nanoscale regimes.

Table1: Comparision Table

parameters / Technologies	Power cosumption	delay	area	Power and delay product
Cmos 45nm	46.551µW	82.05ps	158.9µm2	3.819X10^-15
Cmos 45nm using 6T	4.102nW	75.02ps	16.7µm2	3.077X10^-19
Finfet 7nm using 6T	1.326µw	24ps	0.9µm2	3.1824X10^17

The performance of a low-power 4×1 multiplexer using CMOS 45nm and FinFET 7nm technologies is compared based on key parameters: power consumption, delay, area, and power-delay product (PDP).

Power Consumption:

FinFET 7nm exhibits significantly lower power consumption (1.326 µW) compared to CMOS 45nm (46.551 µW). This demonstrates the superior energy efficiency of FinFET technology.

Delay:

The delay is greatly reduced in FinFET 7nm (24 ps) versus CMOS 45nm (82.05 ps), indicating much faster operation with FinFET.

Area:

FinFET 7nm occupies a much smaller area (0.9 μm²) compared to CMOS 45nm (158.9 μm²), reflecting the higher integration density achievable with FinFETs.

Power Delay Product (PDP):

The PDP for FinFET 7nm (3.182×10^{-17}) is substantially lower than that of CMOS 45nm (3.819×10^{-15}), confirming better overall energy efficiency and performance.

VII. Applications

- Low-power VLSI systems
- High-speed processors
- Signal routing circuits
- FPGA architectures
- Data communication systems

VIII. Conclusion

This paper presented the design and performance evaluation of 2:1, 4:1, and 8:1 multiplexers using FinFET technology. Simulation results confirm that FinFET-based designs provide superior leakage control, improved speed, and lower power consumption compared to conventional CMOS implementations. The results validate FinFET as a promising technology for future low-power and high-performance digital systems.

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