Power Efficient ADC using VCO with Current Mode Logic and Power Gated MOSFETs

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***Abstract*—The increasing demand for power efficient Analog-to-Digital Converters (ADCs) has led to advancements in Voltage-Controlled Oscillator (VCO)-based ADCs. This work presents a VCO-based ADC with a current-starved architecture and power-gated MOSFETs to achieve significant power reduction while maintaining high precision. The design utilizes a seven-stage ring oscillator integrated with power-gating and MOS Current Mode Logic (MCML) techniques to minimize leakage and dynamic power losses. A Frequency-to-Digital Converter (FDC) processes the VCO's frequency modulated output into a digital format, ensuring stability and accuracy. Simulations in Cadence Virtuoso using 45-nm CMOS technology reveals a 97.1% reduction in total power consumption, with dynamic power reduced from 255.3 µW to 26.87 µW (89.5% reduction) and static power reduced from 832.8 µW to 5.02 µW (99.4% reduction) compared to non-power-gated designs. These betterments make the designed configuration highly effective for IoT-enabled systems, low-power signal processing, battery-operated devices, wireless communication, biomedical monitoring, and portable healthcare technologies.**

***Index Terms*—Voltage-Controlled-Oscillator (VCO), Analog-to-Digital Converter (ADC), Frequency to-Digital Converter (FDC), Dynamic Power Consumption, Static Power Reduction.**

I. INTRODUCTION

The growing need for power efficient and compact electronic systems has led to the exploration of alternative ADC architectures, with Voltage-Controlled Oscillator (VCO)-based ADCs emerging as a promising solution. Traditional Analog-to-Digital Converters (ADCs) like Successive Approximation Register (SAR) ADCs and Flash ADCs are widely used due to their high-speed operation and accuracy. However, their high power consumption makes them unsuitable for applications that demand stringent power efficiency, such as portable medical devices, IoT-based health monitoring systems, and low-power communication systems. Unlike conventional ADCs, which rely on voltage or current levels for digitization, VCO-based ADCs convert analog signals into frequency-modulated outputs, which are then processed digitally. This frequency-domain approach enhances power efficiency, scalability, and precision, making it well-suited for modern electronic systems.

The Voltage-Controlled Oscillators, especially current-starved variant have emerged as a preferred choice due to their precise frequency modulation and low power consumption [1]. By limiting the current flow through each stage of the oscillator, current-starved VCOs achieve fine-tuned frequency control, which is crucial for systems requiring high accuracy. Power gating significantly reduces leakage currents during idle states, ensuring efficient power use, while CML reduces dynamic power losses and ensures high-speed operation with minimal noise, making these designs particularly suitable for noise-sensitive and portable applications[2]. The incorporation of Frequency-to-Digital Converters (FDCs) in VCO-based ADCs machinate challenges such as voltage-to-frequency nonlinearity. FDCs convert the frequency-modulated signals from the VCO into precise digital outputs, ensuring high accuracy and robustness. The modularity of VCO-based ADCs makes them adaptable for various applications, enabling scalability and integration with advanced technology nodes, including 45-nm, 130-nm, and 180-nm CMOS processes. These advancements have contributed to significant reductions in power consumption, area and noise while improving overall performance. As CMOS scaling continues to advance, these designs are becoming even more relevant, addressing the growing demand for robust and power efficient systems across various domains. The ability of VCO-based ADCs to combine low power consumption, high accuracy, and compact design positions them as a vital technology for next-generation electronics [3].

II. RELATED WORKS

A non-power gated VCO operates continuously without mechanisms to isolate inactive circuit blocks, leading to significant leakage and dynamic power consumption from **Figure.1**[4]. While it provides stable oscillation for frequency generation, the lack of power-gating results in higher power loss during idle states, making it less suitable for power constrained applications as explained in the **Table 1**. This inefficiency is particularly evident in portable systems, where reducing power consumption is critical.

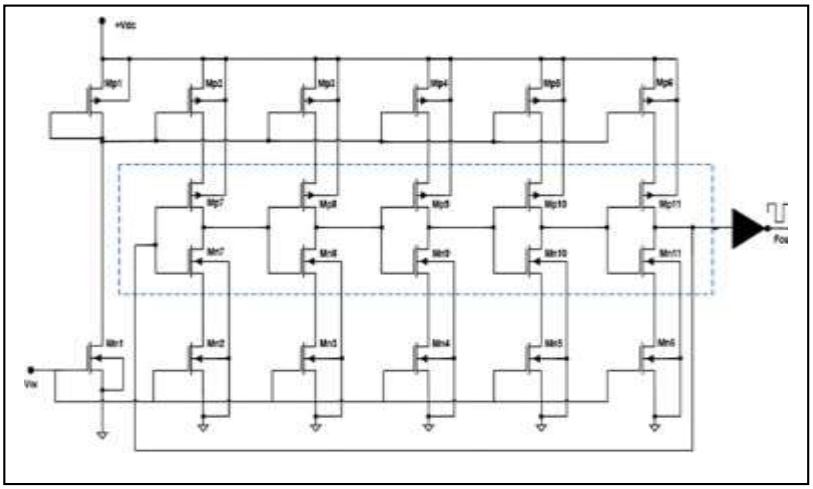

Figure 1. Non-Power Gated VCO

Table 1
Operation of Non-Power Gated VCO ADC

Phase	Transistor State	Operation
Startup	Mp1, Mn1 ON, others OFF	Circuit initializes and prepares for oscillation.
Charging Phase	Mp2-Mp6 ON, Mn2-Mn6 OFF	PMOS transistors allow capacitors to charge.
Discharging Phase	Mp2-Mp6 OFF, Mn2-Mn6 ON	NMOS transistors enable capacitor discharge.

III. PROPOSED METHODOLOGY

3.1 Power Gated VCO

The Voltage-Controlled Oscillator (VCO) serves as the core of the ADC, converting the analog input voltage into a frequency-modulated signal. Its design incorporates several key techniques to optimize power efficiency and performance. The current-starved architecture limits the current flow through each inverter stage in the ring oscillator, enabling precise control over the oscillation frequency while reducing dynamic power consumption. To further enhance efficiency, power-gated MOSFETs isolate the circuit from the power supply during idle states, significantly minimizing leakage power, which is particularly beneficial for devices with long idle periods shown in the **Figure 2**[5].

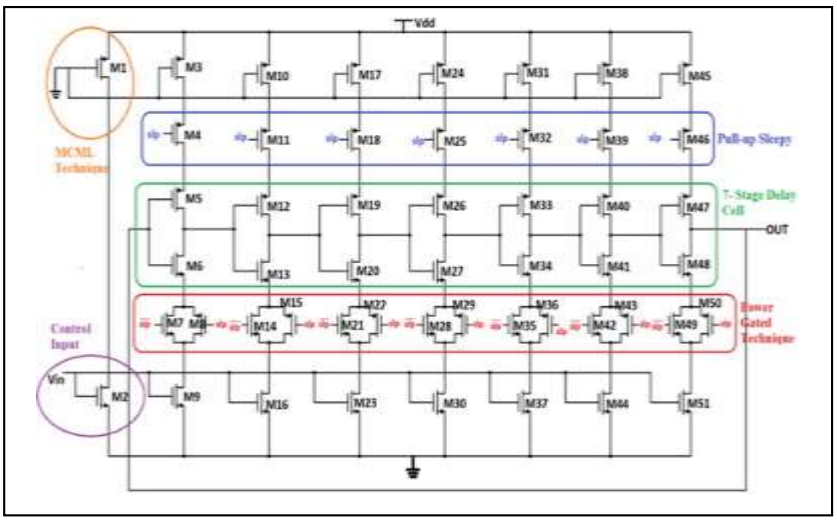

Figure 2. Power Gated VCO

Table 2
Operation of Power Gated VCO

Phase	Transistor State	Operation
Initialization	M1, M2 ON; Others OFF	Power is supplied, but oscillation hasn't started.
Sleep Mode	All transistors OFF	Sleep transistors cut power, reducing leakage.
Power Gating ON	M7-M50 ON; M1, M2, SLP OFF	Power-gated transistors activate, allowing oscillation.
Charging Phase	PMOS ON; NMOS OFF	Capacitors charge, preparing for switching.
Discharging Phase	NMOS ON; PMOS OFF	Capacitors discharge, completing the cycle.
Power-Off Mode	All transistors OFF	Sleep transistors disable power, reducing power consumption.

Additionally, pull-up sleepy transistors help conserve power by partially disconnecting inactive circuit regions, thereby reducing static power consumption explained in the **Table 2**. The inclusion of Current Mode Logic (CML) ensures consistent current flow, which minimizes switching power losses. Unlike conventional CMOS logic, CML operates with smaller voltage swings, leading to lower dynamic power consumption and minimal noise. This makes CML particularly suitable for high- speed, low-power applications.

3.2 Frequency to Digital Converter

The FDC converts the VCO's frequency-modulated output into digital values. It uses a resettable counter to measure the number of oscillation cycles within a predefined time interval [4] [8] [9] [10] [11] [12]. The resulting digital code corresponds to the input control voltage applied to the VCO, ensuring accurate and monotonic signal conversion.

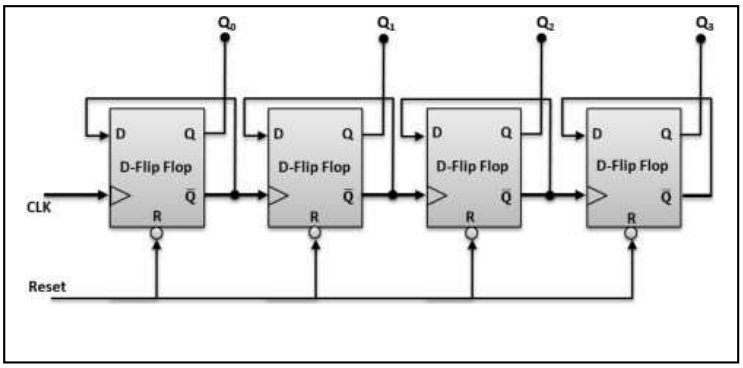

Figure 3. Block diagram of frequency to digital converter

The FDC's output reflects the input frequency, with minimum input voltage producing a single count ([D3D2D1D0 = "0001"]) and maximum input voltage generating 16 counts ([D3D2D1D0 = "1111"]) as shown in the **Figure.3**. Its compact design, power efficiency, and robust reset mechanism make it ideal for high-speed and precise frequency-to-digital conversion tasks.

IV. RESULTS AND DISCUSSION

4.1 Non-Power Gated VCO

The waveform shown in the **Figure 4** represents the output signal of a Non-Power Gated VCO, showing continuous oscillation with higher power consumption.

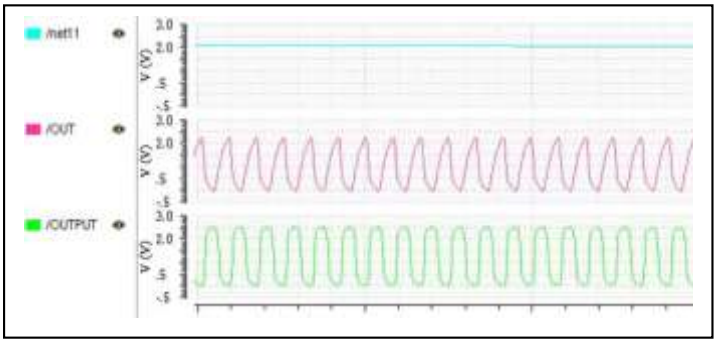

Figure 4. Waveform of Non-Power Gated VCO

4.2 Power Gated VCO

The waveform shown in the **Figure 5** illustrates the output of a Power Gated VCO, demonstrating stable oscillations that minimizes power consumption.

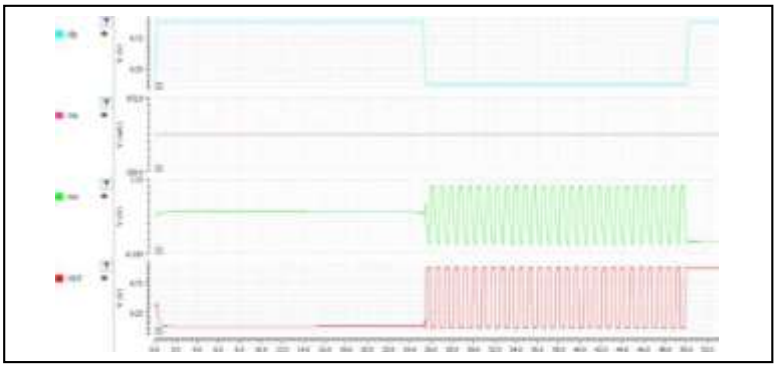

Figure 5. Waveform of Power Gated VCO

4.3 Control Voltage Vs Frequency

The working frequency range of the Power Gated VCO is 0.605 GHz to 1.39 GHz, depending on the input control voltage and circuit parameters at varied supply voltage VDD ranging from 0.8 V, 1 V,1.2 V. The integration of power gating techniques helps maintain stable oscillations while reducing power consumption shown in the **Figure 6**.

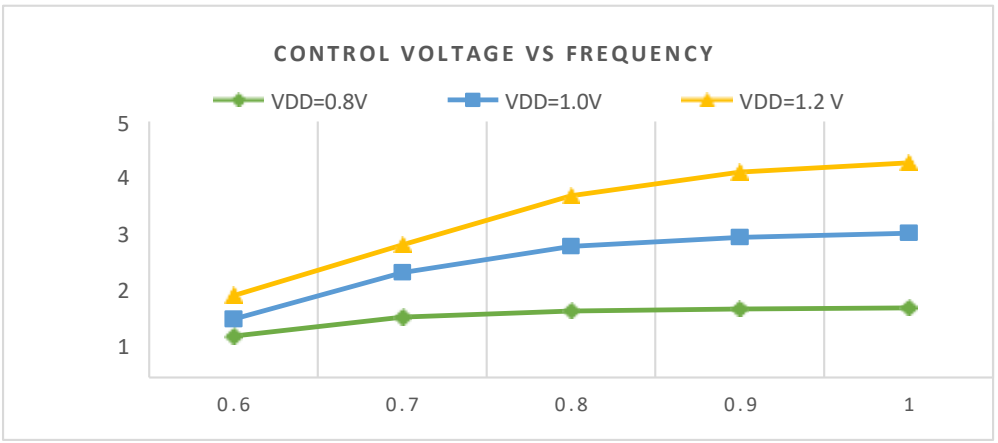

Figure 6. Control Voltage Vs. Frequency for Different VDD Levels

4.3 Frequency to Digital Converter

The waveform shown in the **Figure 7** illustrates the output of the FDC, showcasing the digital representation of the VCO's frequency-modulated signal.

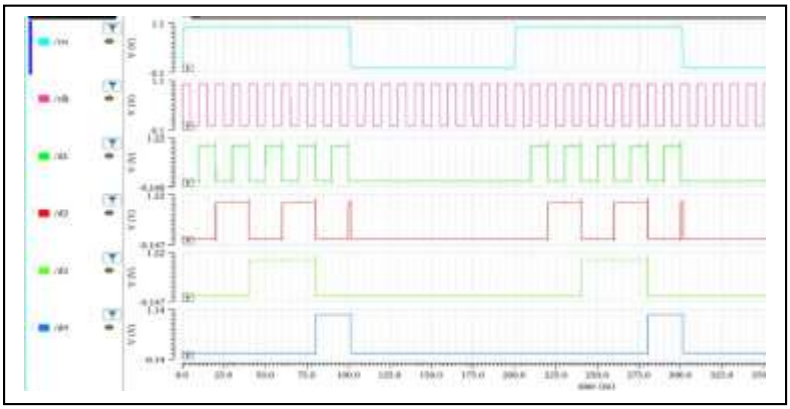

Figure 7. Frequency to Digital Converter

4.4 Non-Power Gated VCO Based ADC

The waveform of a Non-Power Gated VCO-Based ADC shows continuous oscillations, leading to higher power consumption due to the absence of power-gating techniques shown in the **Figure 8**.

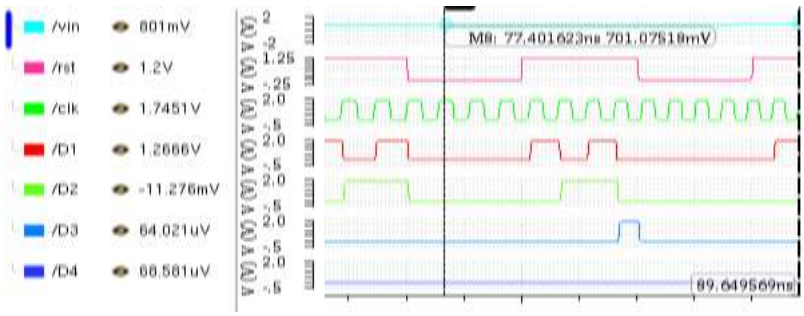

Figure 8 Waveform of Non-Power Gated VCO at VIN=0.8 V

4.5 Power Gated VCO based ADC

The waveform of a Power Gated VCO-Based ADC demonstrates reduced power consumption by entering low-power states during idle periods, enhancing power efficiency as shown in the **Figure 9** and **Figure 10** .

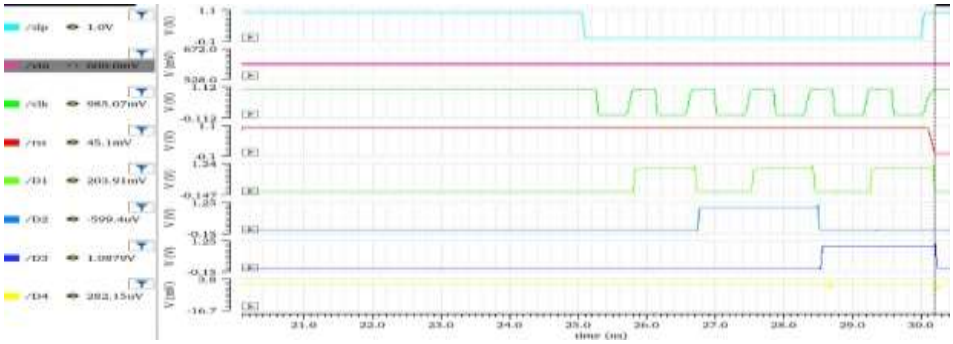

Figure 9 Waveform of Power Gated VCO at control voltage VIN = 0.6 V

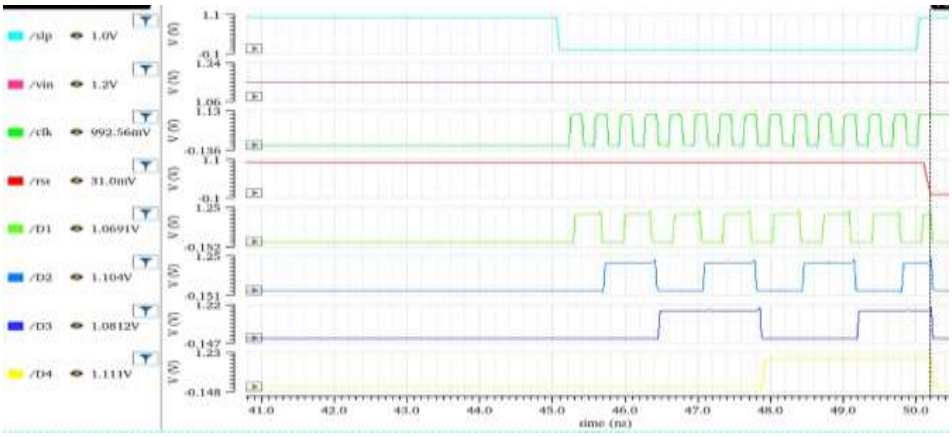

Figure 10 Waveform of Power Gated VCO at control voltage VIN = 1.2 V

4.6 Control Voltage Vs Digital Output

The **Figure 11** shows how the digital output varies with the control voltage in the ADC, ensuring a consistent and accurate conversion process.

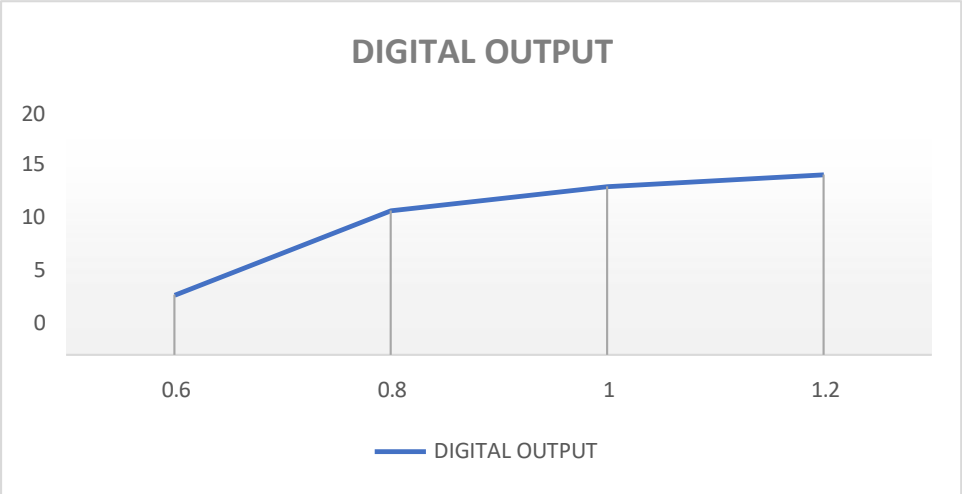

Figure 11 Control Voltage Vs Digital Output Analysis

Table 3

Power Comparison between Power Gated and Non-Power Gated VCO-ADCs

Parameter	Power Gated VCO-ADC	Non-Power Gated VCO-ADC	Power Reduction (%)
Static Power (µW)	5.02	832.8	99.4%
Dynamic Power (µW)	26.87	255.3	89.5%
Total Power (µW)	31.89	1088.1	97.1%
Power Efficiency	High	Low	–

Static power is reduced by 99.4%, making the Power Gated VCO-ADC highly efficient in standby mode as shown in the **Table 3**. Dynamic power is reduced by 89.5%, improving active power consumption. Total power consumption is reduced by 97.1%, ensuring a significant power-saving advantage. These improvements make the power-gated VCO -ADC highly suitable for low-power applications such as biomedical and IoT-based systems.

Table 4

Performance Comparison Across Different Technology Nodes

	Process(nm)	Supply Voltage (V)	Power (mW)
[4]	130	1.2	0.257
[13]	180	1.8	24
[15]	130	1.2	0.24
This Work	**45**	**1**	**0.026**

Table 4 highlights the impact of CMOS scaling on power consumption. As the technology node shrinks from 180 nm to 45 nm, power usage decreases significantly. The proposed 45 nm design (1V) consumes only 26.87 µW, achieving a 97.1% reduction in total power. This improvement is due to the integration of power-gating and current-starved techniques, which minimize leakage and dynamic power. The results confirm that the design is highly efficient for low-power applications.

V.CONCLUSION

This work presents a Power Gated VCO-based ADC with a current-starved architecture, designed to achieve significant power reduction while maintaining high precision. By integrating Power Gated MOSFETs and MOS Current Mode Logic (MCML), the proposed design effectively minimizes leakage and dynamic power losses. The implementation of a seven-stage ring oscillator enhances frequency stability, while the Frequency-to-Digital Converter (FDC) assured accurate signal conversion. Simulations conducted in Cadence Virtuoso using 45-nm CMOS technology demonstrate a 97.1% reduction in total power consumption, with dynamic power decreasing from 255.3 µW to

26.87 µW (89.5% reduction) and static power dropping from 832.8 µW to 5.02 µW (99.4% reduction) compared to conventional Non-Power Gated designs. The significant power savings and improved efficiency make the designed architecture apt for power-efficient embedded systems, real-time sensing applications, medical signal acquisition, wearable technology, and low-power industrial automation. Its scalability confirm adaptability to future low-power electronic applications, making it a promising solution for next-generation smart devices and intelligent monitoring systems.

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