POWER REDUCTION IN DOMINO LOGIC USING CLOCK GATING IN 16NM CMOS TECHNOLOGY

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Abstract

Power consumption is a serious issue in today's VLSI circuit design, especially in deep-submicron technologies. CMOS NAND logic and domino logic are two popular design styles, each with different power consumption behaviors. Historically, domino logic has been regarded as power-consuming as a result of constant clock switching. Still, our simulation output for a 16nm CMOS process demonstrates that domino logic is power-consuming (2.05 µW) versus CMOS NAND logic (3.8 µW). It saves 46.05% power when implementing domino logic rather than dynamic CMOS NAND logic and domino logic versus dynamic CMOS Nand logic static power saving is 99.99%.

In order to compare more thoroughly the influence of the style of logic on power, we compare the 1-bit and 4-bit full adders. From the results, it is apparent that the domino logic's power benefit does not vary for circuits of various complexities. Power reduction is realized by having fewer transistors, less switching capacitance, and an enhanced charge-sharing technique in domino logic. These results indicate that domino logic can be used as a power-efficient alternative for high-speed, low-power digital circuit designs in advanced CMOS technology nodes.

Keywords- Staic, Dynamic, CMOS, Domino logic, Clock gating.

1.INTRODUCTION

As CMOS technology is reduced to ultra-deep-submicron and deep-submicron nodes, power consumption has emerged as a key issue in VLSI circuit design. As supply voltage, device size, and threshold voltages continue to decrease in a persistent manner, leakage currents have risen, contributing significantly to static power dissipation. Dynamic power used to be predominant over static power in larger technology nodes (>350nm), but in sub-100nm.technologies, static power dissipation has emerged as a serious issue.

Domino logic has received considerable interest in VLSI design because of its high-speed operation and less space than in static CMOS. In contrast to static CMOS logic, which uses complementary transistors for every logic function, domino logic employs a precharge-evaluate technique and is therefore faster and more efficient for high-performance designs. Nevertheless, the domino logic's continuous clock switching results in higher power dissipation, especially in standby mode. Several methods have been suggested to counter this problem, including low-swing clocking, supply voltage scaling, and clock gating.

This work targets power comparison between static and dynamic power of domino logic and CMOS NAND logic in a 16nm CMOS process, targeting 1-bit and 4-bit traditional full adders. Our simulation results prove that domino logic uses less power (2.05 µW) than CMOS NAND logic (3.8 µW), realizing a 46.05% reduction in dynamic power as same as 4-Bit conventional full adder uses less power compared to 1-Bit realizing a 60% reduction in dynamic power. The findings contradict traditional assumptions regarding domino logic as power-hungry and demonstrate its potential as a low-power alternative in contemporary VLSI design. Additional examination of full adder circuits validates the consistent power savings of domino logic over CMOS NAND logic.

2. EXISTING METHOD

1. CMOS NAND Logic

A CMOS NAND gate is constructed out of PMOS and NMOS transistors. The number of the transistors utilized follows this general rule: for a NAND gate is made out of The pull-up network and two series NMOS transistors is made out of two parallel PMOS transistors.

Structure and Operation:

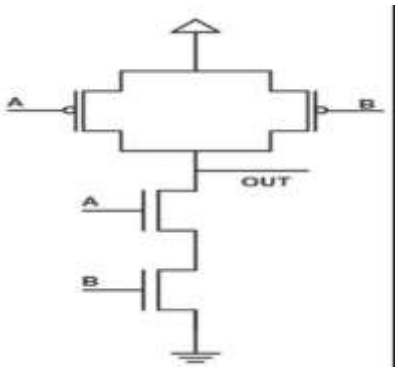

Fig.1. Basic CMOS NAND Circuit

Pull-Up Network (PUN):

• Constructed by connecting parallel PMOS transistors.

•Ensures the output to be HIGH (1) unless all inputs are HIGH.

The Pull-Down Network (PDN):

•PDN is constructed by connecting NMOS transistors in series.

•Guarantees that only when all of the inputs is high will LOW (0) is the output.

Truth Table:

A	B	OUTPUT(Y)
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 2. NAND Truth table

Power Dissipation issues:

• Ongoing switching of the clock results in dynamic power consumption at high levels.

• A pulse-shaped output ensures higher power usage in standby.

1-Bit Traditional full adder

• A 1-bit full adder is an elementary arithmetic building block that calculates the sum of three binary input: A,B and Carry-in(Cin).

• Boolean Equations:

• Sum (s) = A ⊕ B ⊕ Cin

•Carry out (Cout)= AB + BCin + ACin

• The traditional 1-bit full adder is implemented using dynamic logic gates, which are:

• AND gates for generating carry. XOR gates for generated sums. OR gate for output in final carries

• Takes advantage of clock gating to enhance power efficiency.CMOS NAND Logic and Full Adder 1-bit in domino logic are power-hungry due to constant clocking.

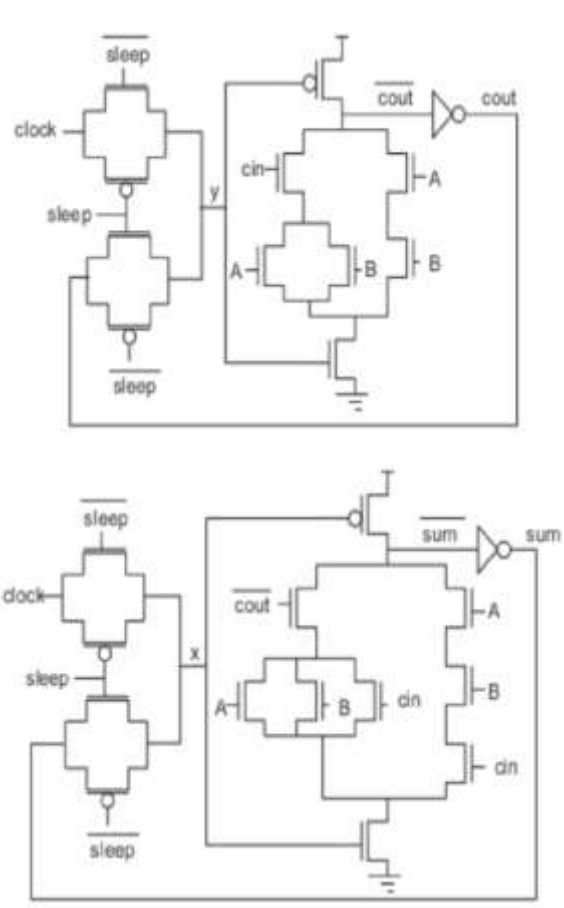

Fig. 3. A 1-bit conventional full adder circuit

3. PROPOSED METHODOLOGY

- 2 Input nand gate using Domino logic

Domino logic is a changeable logic family used in high-speed VLSI circuits. It operates in 2 phases:

1. Phase of Precharge (Clock = 0)

The dynamic A PMOS transistor charges node (X) to VDD. The output remains low until evaluation.

2. Phase of Evaluation (Clock = 1)

If the pull-down network (PDN) does conduct (i.e., inputs permit discharge), X, the dynamic node, discharges to zero, generating an output of 1.If the PDN doesn't conduct, the dynamic node maintains its precharge value (1), and the output remains low

Limitations of Standard Domino Logic

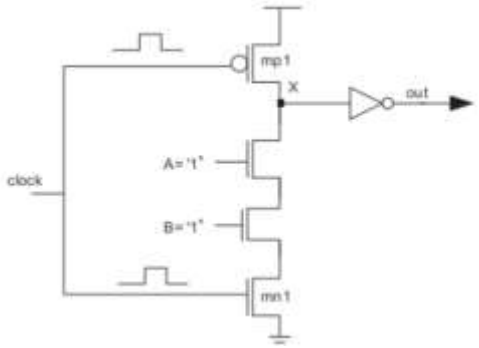

Fig. 4. 2 Input nand gate using domino logic

- 4-Bit Conventional Full Adder

A full adder 4-bit is an analog digital circuit used in 4-bit two numerical addition. It consists of four cascaded 1-bit full adders, where the carry output of one stage is fed as the carry input to the next stage. The primary function of this circuit is to add Provide a 4-bit sum and carry using two 4-bit binary numbers and a carry input. Each 1-bit full adder contains 2x1 multiplexer to reduce the power.

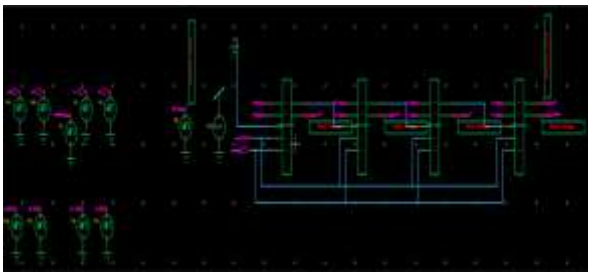

Fig . 5. 4-Bit Full Adder Block diagram

4. THE PROPOSED METHODOLOGY IMPROVES POWER EFFICIENCY BY INTRODUCING

Clock Gating: Prevents the clock to switch when inputs don't change.

In Domino Logic, circuits go through two different phases:

a. Precharge Phase: Clock State: when the clock reads zero.The node that is dynamic (X) is precharged to (logic high, '1') by a PMOS transistor.The NMOS pull-down network (PDN) is OFF, so it does not discharge. The output is stable.

Purpose: Causes the node to be precharged prior to entering the evaluation phase.

Example in a 4-bit Full Adder (Domino Logic): Every component of the adder has a precharge circuit.. When, all dynamic nodes (X0, X1, X2, X3) are precharged to logic high (1).Carry propagation circuits are also precharged.

b. Evaluation Phase: Clock State: Once the clock () is high (1).Operation The Nmos transistor and the Pmos transistor are both off. pull-down network (PDN) is ON.

In the event that the inputs are such that the PDN carries, the node discharges to 0.Otherwise, the node keeps its precharge value.

Purpose: Computes the final output of the circuit.

Example in a 4-bit Full Adder (Domino Logic): When sum bits are required to be '1', the dynamic node stays charged. When sum bits are required to be '0', the dynamic node is discharged via the NMOS network.

Output Hold Circuit: Maintains the previously computed output, precluding unnecessary transitions. Output hold is a term used to describe a circuit's capability to hold its output value even when the inputs no longer change. Output hold is crucial in a 4-bit adder in applications where the adder must have its sum and carry outputs maintained while precluding unnecessary transitions that consume power.

Advantages of Output Hold:

- Prevents Unnecessary Power Consumption: Prevents continuous enabling and disabling of outputs.
- Improves Stability: Provides stable output even if the inputs are no longer changing.
- Decreases Switching Activity: Essential in low-power VLSI designs such as Domino Logic adders.

3. Multiplexer (MUX)-Based Clock Control:

Utilizes a 2:1 MUX to switch from the clock signal to the output. A 2:1 multiplexer is employed to switch between the newly computed output and the old value stored.

5. IMPEMENTATION&SIMULATON

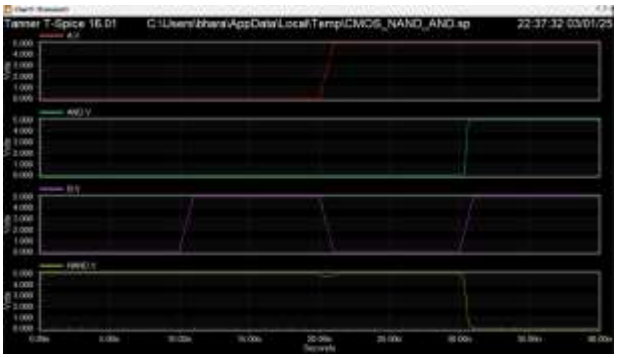

Fig. 6. Output of CMOS NAND Logic

Power Dissipation in Simple CMOS NAND Logic: The specified power dissipation is 3.8 µW. Dynamic power is predominantly responsible for the total power consumption, largely because of repeated switching actions.

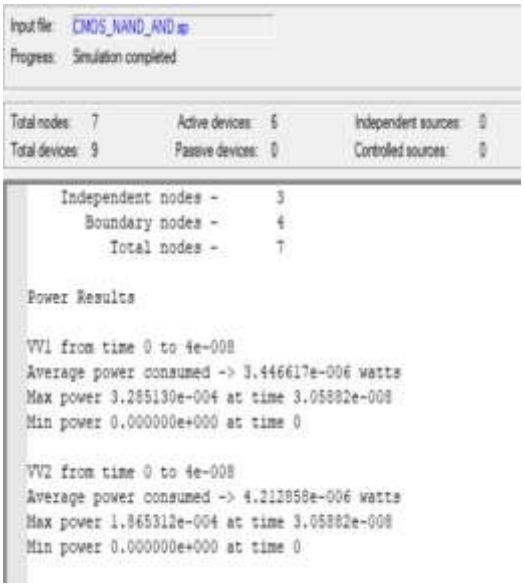

Fig. 7. Power utilization of Basic CMOS NAND Logic.

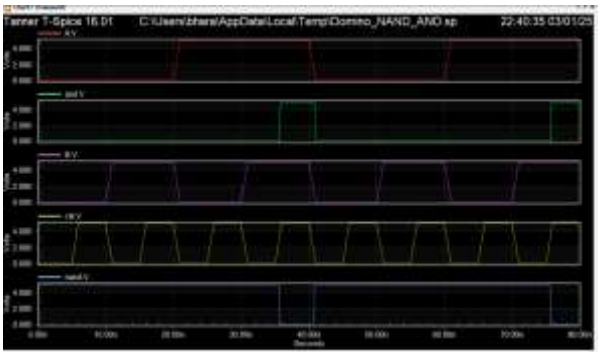

Fig . 8. Output of 2-bit NAND Using Domino Logic.

Power Dissipation in Domino Logic: The power dissipated is 2.05 µW, less than simple CMOS NAND logic.This is mainly because of efficient circuit design and clock gating methods.Dynamic power reduced results in less overall power dissipation, thus the circuit becomes more energy- efficient.

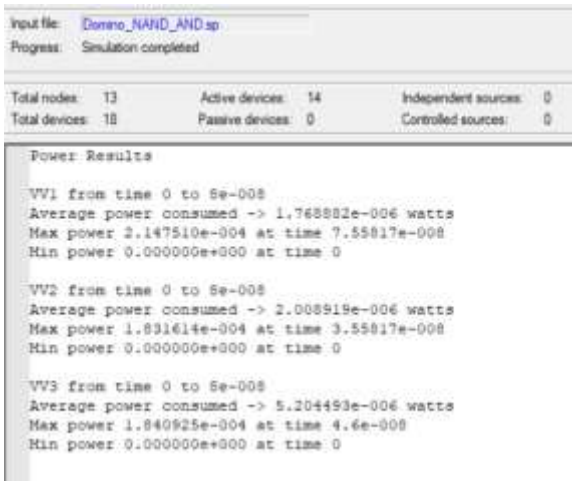

Fig.9. Power Utilization of 2-Bit NAND Using Domino Logic.

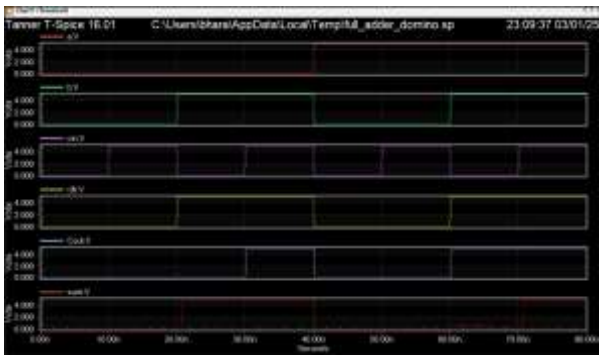

Fig. 10. Output of 1-Bit conventional Full Adder

Power Consumption in 1-Bit Full Adder: The total power consumed is 15 µW.This increase is due to the complexity of the circuit, involving multiple logic gates.

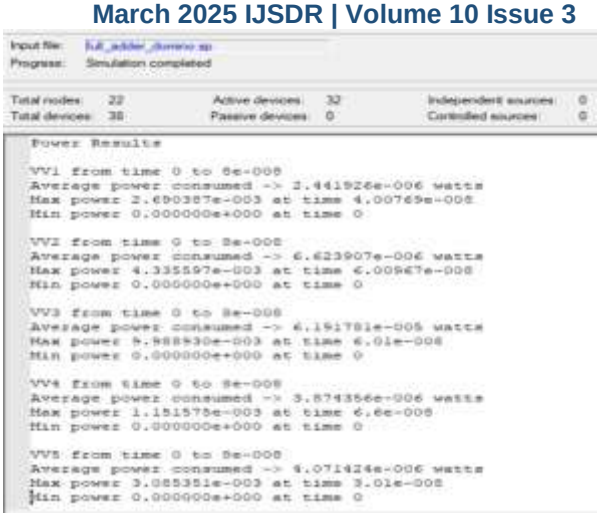

Fig.11. Power utilization of Full Adder 1-Bit conventional.

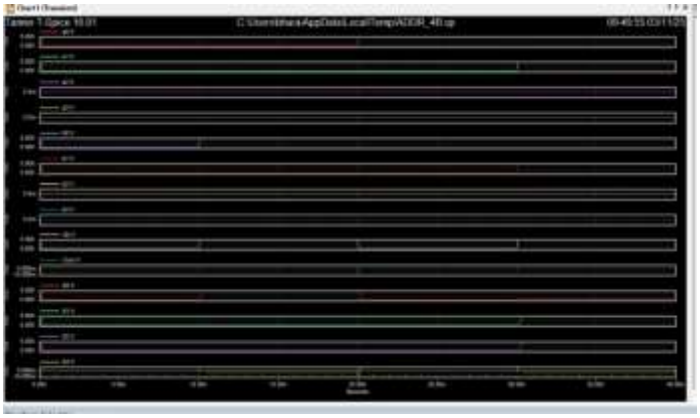

Fig. 12. Output of 4-Bit conventional Full Adder

- **Power Consumption in 4-bit full adder**: The total power consumed is 24 µW.This methodology improves the power efficiency by introducing
- Clock gating
- Output hold circuit
- Mux based clock control

6.**COMPARISON**

TABLE I

Logic Type	Power Consumption (µW)	Percentage of Original power(%)
CMOS NAND Logic	3.8	100
Proposed Domino Logic	2.01	52.9
Power Reduction	1.79	47.1

This Table .I shows that proposed Domino Logic reduces power consumption by 1.79uW, which is a 47.1% reduction compared to the CMOS NAND Logic.

TABLE II

Full Adder Type	Power Consumption (µW)	Percentage of Expected Power (%)
1-bit Conventional Full Adder	15	100
Expected 4-bit Conventional FA	60	100
Proposed 4-bit Conventional FA	24	40
Power REduction	36	60

This Table II. shows that proposed 4-bit full adder reduces power consumption by 36 µW(60%).

7.Conclusion

In conclusion, CMOS domino logic provides high-speed operation with reduced area compared to static CMOS logic. However, its continuous clock switching leads to significant power dissipation. Clock gating in domino logic, especially in circuits like 1-bit and 4-bit conventional full adders, effectively reduces static and dynamic power consumption by bypassing the clock during standby mode while retaining circuit state.The proposed technique achieves substantial power savings, making it suitable for low-power applications in ultra-deep submicron technology.

8.References

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