When the Signal Changes Return Plane and its Mitigation Methods

Bhargav Dharmendra Chauhan[1], Guariech Ishaan Pilla[2], Taher Ujjainwala[3]

[1,2,3]Graduate Student
Electrical Computer and Energy Engineering
University of Colorado Boulder, Colorado, United States

Abstract: In this paper, we investigate the effects of signal transitions between layers in a 4-layer printed circuit board (PCB) with a stack-up of signal-ground-ground-signal (S-G-G-S) . We observe impedance changes and cavity noise, leading to ground bounce when the signal transitions from the top layer to the bottom layer [1]. To mitigate these effects, we examine the difference in crosstalk when the return path for the signal is present and when it is removed. We use a high-frequency structure simulator (HFSS) and Advanced Design System (ADS) to simulate and model the system in frequency domain, extract S-parameter data, and plot graphs to verify our results. The main objective of this project is to demonstrate the importance of proper return path design for high-speed signals in multi-layer PCBs.

Keywords: Printed Circuit Board, Signal Integrity, Ground Bounce, Cavity Noise, HFSS, ADS

I . INTRODUCTION

Printed circuit boards (PCBs) are widely used in electronic devices, and signal integrity is a critical issue when designing PCBs. In high-speed electronic systems, the return path for a signal is as important as the signal path itself. When the signal transitions from one layer to another [1], the impedance of the return path can change. This can lead to a ground bounce, which is a transient voltage that can cause signal degradation. In this paper, we focus on the effects of signal transitions between layers in a 4-layer PCB with a stack-up of signal-ground-ground-signal (S-G-G-S) [1][2]. We observe that when the signal transitions from the top layer to the bottom layer, impedance changes and cavity noise occur, resulting in ground bounce. Ground bounce can lead to signal integrity issues, such as increased crosstalk [3] and reduced signal-to-noise ratio. To mitigate these effects, we investigate the difference in crosstalk when the return path for the signal is present and when it is removed. There are a number of methods for mitigating ground bounce. One method is to use a return via close to the signal trace. A return via is a small conductor that connects the signal trace to the return plane. The return via provides a low-impedance path for the return current, which helps to reduce ground bounce [5]. We use HFSS and ADS to simulate and model the system in the frequency domain, extract S-parameter data, and plot graphs to verify our results. Our study contributes to a better understanding of signal integrity issues in PCB design and provides insights into mitigation methods for ground bounce.

A via is a conductive hole that connects different layers of a PCB. However, a via also introduces some parasitic capacitance [3] [6] and inductance, which can cause impedance discontinuity [6] and voltage drop along the signal path. When a signal changes from a layer with a reference plane (such as a ground plane) to a layer without a reference plane, the return current of the signal has to find another way to flow back to the source. This creates a loop area between the signal trace and the return path, which can act as an antenna and radiate EMI. Moreover, the return current can induce noise voltage between different reference planes due to their parasitic capacitance. Ground bounce is the voltage created on the ground return conductor due to changing currents through the total inductance of the return path. It is the primary cause of switching noise and EMI [6].

Ground bounce can have serious consequences for high speed signals, such as increasing the logic noise margin, reducing the signal-to-noise ratio (SNR), creating false triggering or glitches, and increasing crosstalk between adjacent traces. Therefore, it is essential to minimize ground bounce by designing proper return paths for high-speed signals in multi layer PCBs. One of the effective methods to reduce ground bounce is to place a return via close to the signal via [8], so that the return current can follow the signal current closely and minimize the loop area. This can also reduce the impedance discontinuity and EMI radiation caused by vias.

We aim to demonstrate the effects of signal transitions between different layers of a four-layer PCB with a stack-up of S-G-G-S. We use HFSS to model and simulate the PCB and observe the impedance change and cavity noise (voltage) between the planes when the signal changes from the top
layer to the bottom layer. We also study the difference when there is a return via close to the signal trace. Once the HFSS model is simulated, we plan to verify our results by importing the S-parameter data from HFSS to ADS Keysight simulation tool and plotting the graphs. We also compare our results with theoretical methods and apply rule 9 which states ”Never do a measurement or simulation without first anticipating what you expect to see” [7].

II. LITERATURE SURVEY

[2] The paper discusses the challenges of designing modern electronic systems, which require smaller form factors, complex functionalities, higher speeds, and greater reliability. As a result, printed circuit boards (PCBs) are becoming more densely populated with multiple integrated circuits (ICs) and voltage supplies. This creates issues with crosstalk and electromagnetic (EM) emissions, which can affect signal integrity (SI) and power integrity (PI) and lead to failed electronic systems.
To address these issues, a novel power delivery method using impedance-controlled transmission lines called power transmission lines (PTLs) is proposed. This method has been shown to reduce the effect of return path discontinuities (RPDs) that arise from signal traces changing routing layers through vias.
The paper presents a comparison of coupling from an aggressor signal line making via transitions to an adjacent victim signal line on three different 4-layer PCB test vehicles: GP (ground-power), PG (power-ground), and PTL. The results show that the PTL-based design demonstrated lower wide-band coupling and significantly lower power supply noise than the other two plane-based test vehicles when running gigabit pseudo-random binary sequence (PRBS) signals.
We can use this paper to identify any issues with RPDs and determine whether a PTL-based PDN design could be more effective than a traditional power and ground plane design, we can use this proposed PTL-based PDN design to deliver power to high-speed switching loads, which can help improve signal and power integrity by reducing the effect of return path discontinuities

[3] This paper is about investigating the crosstalk problem among vias in high-speed digital circuits on printed circuit boards (PCBs). Crosstalk is an unwanted noise signal coupled from one signal to its adjacent signal (here, from the signal from one via to another via) that can significantly affect the integrity of high-speed signals.
The paper proposes a physics-based equivalent circuit model to study the underlying mechanism of crosstalk among vias as a function of various geometrical parameters, including parallel plane pair thickness, layer count in the PCB stack up, ground via patterns, and parallel plane pair dimensions.
The paper also proposes a multi-step crosstalk evaluation procedure based on the study for PCB layout design verification. The study provides a quantitative relationship between crosstalk level and different geometrical parameters, which can be used for practical PCB layout design verification.
Applying this knowledge to our project may involve developing a model that characterizes the impedance and capacitance of the relevant components in our circuit, such as the vias, return planes, and signal traces. Once we have a model, we can use it to analyze the crosstalk behavior of our circuit as a function of various layout design parameters. One of the learning of this paper is to use a shorting beside every signal via.

[1] The scope of electronics and miniature design is increasing day by day. When the package size decreases, electronics are packed or developed with multi layer PCB stack-ups that provide higher density. With high density and multi layer PCBA’s micro strip lines are used and it commonly changes signal layers to develop an embedded product. High-speed signals that propagate down the transmission line need to have a return path for the signals. Return current goes hand in hand with the signal propagating down the TL.
Signal changes planes/layers with the help of via. These vias may pass from multiple layers, it may either be ground, power, or any other signal. It is equivalent to understanding the impedance of the signal that propagates down the TL. Vias doesn’t have constant impedance, it adds slight discontinuity. When the stack of S-G-G-S is done and when the signal transitions from the top signal to the bottom signal layer, there are two ground planes in between to return current paths. Here, we will observe and analyze the impact of having a low impedance return current paths for signal transitioning from top to bottom layer. We will also observe the impact when there is via for return current passing through a low impedance path near the signal layer and when there is no vias close to the signal layer.

III. SYSTEM ANALYSIS - PCB MODEL AND SIMULATION SETUP

A. Design Specifications

- 4-layer PCB, Signal-Ground-Ground-Signal
- HFSS simulation, Augmented by ADS
- Board Size = 1 x 0.5 Inch
- Trace Width = 18 mils
- Trace Height = 1.4 mils
- Dielectric Height = 10 mils
- Ground layer Height = 3 mils
- Length (top and bottom) = 0.5 inch
- Via Radius = 13 mils
- Via Pad Radius = 25 mils
- Anti Pad Radius = 35 mils
- FR4 substrate, 1oz copper

B. Simulation Models

We developed three models to demonstrate and simulate the setup using the design specification mentioned above.

1) The first simulation model is four return vias placed close and symmetrically around the via. This provides the best results in terms of reducing reflections, crosstalk, delay, and noise. This is because having multiple return vias would provide a more robust and low impedance path for the signal return current, minimizing the effects of the impedance mismatch.

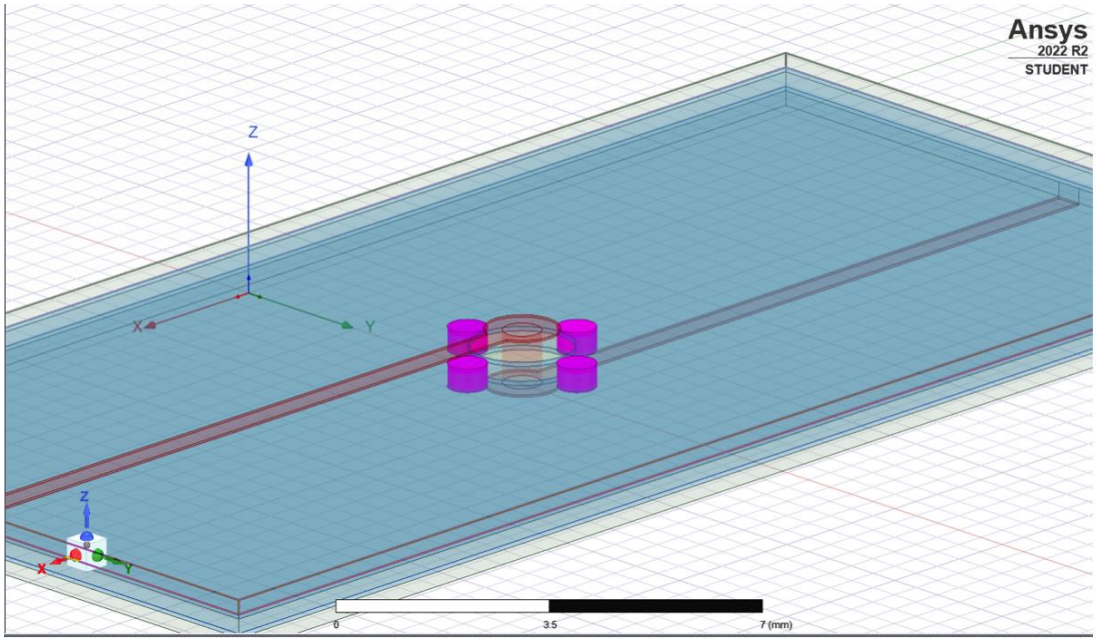

Figure 1: 4 Return Via Setup

2) The second simulation model is only one return via placed close to the via. This model would still provide some benefits in terms of reducing the effects of signal transitions, but it may not be as effective as the first model. This is because having only one return via may not provide enough low-impedance path for the signal return current, leading to potential noise and interference issues.

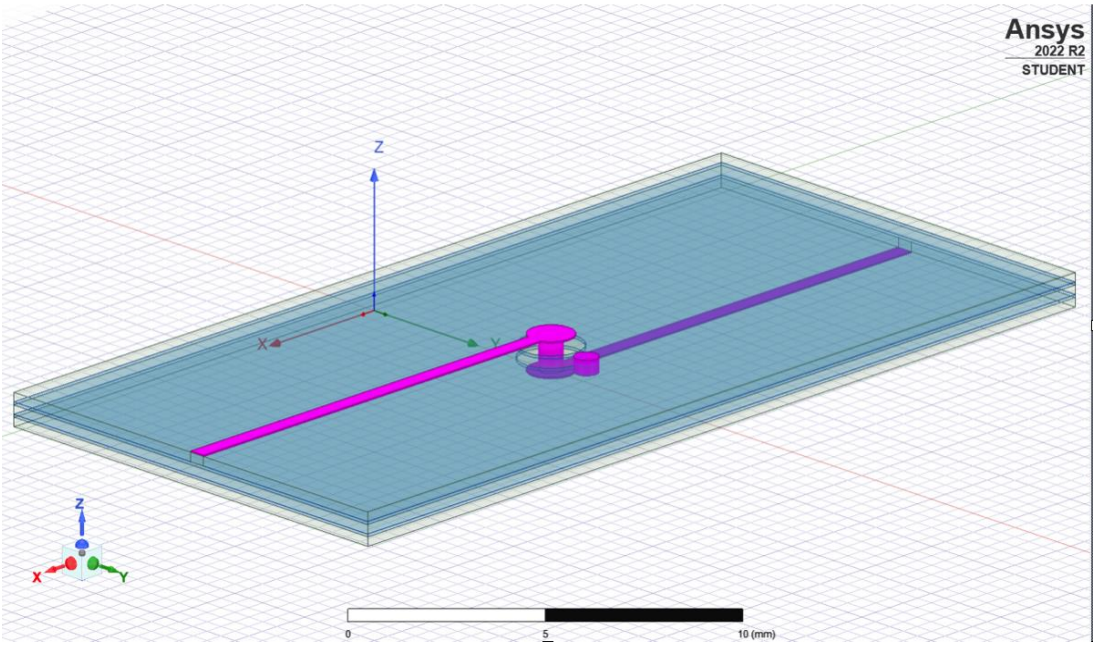

Figure 2: 1 Return Via Setup

3) The Third simulation model is no return via placed closed to Via. This model would likely have the worst performance in terms of signal integrity. This is because without a low-impedance return path for the signal current, reflections, crosstalk, delay, and noise can all become significant issues.

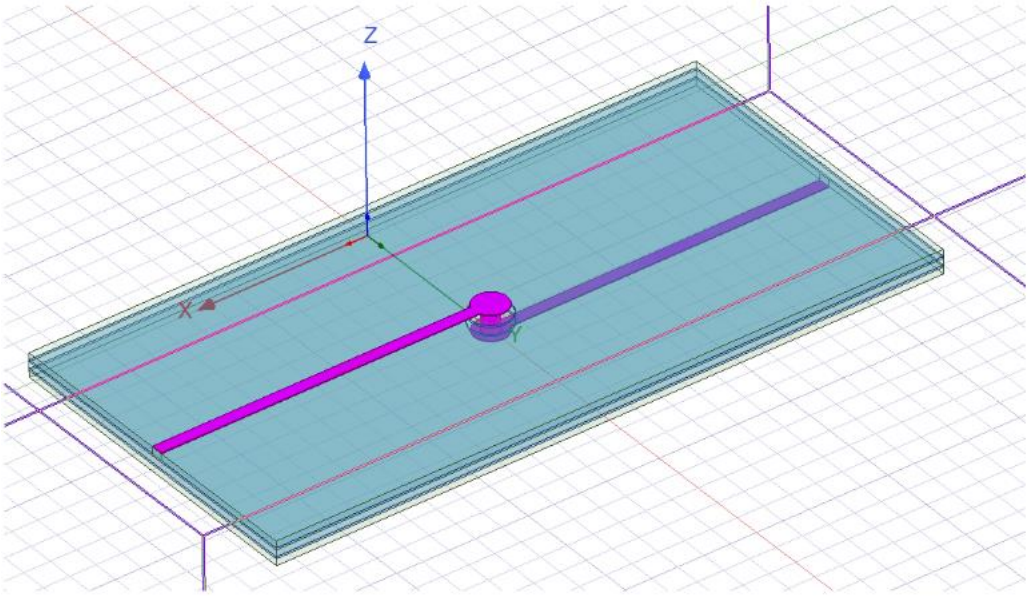

Figure 3: No Return Via Setup

IV. SYSTEM VALIDATION PART 1 - SIMULATION AND OBSERVATION

The simulations below represent the cavity noise. Cavity noise is a type of electromagnetic interference (EMI) that can occur in a 4-layer PCB when a signal transitions between layers with the help of a via. This noise is generated due to the presence of a cavity or resonant structure between the signal via and the adjacent planes [6]. We can observe the difference between No return Via and 4-return via the board. The cavity noise is significantly reduced in 4-return via the board due to adjacent path for return current flowing in the adjacent ground planes.

A. No Return Via

This is the cavity noise observed when no return via is present. As you can see there is a significant amount of cavity noise present because there is no return via present. When the signal transitions from the top to the bottom layer, we can also observe impedance change when the via is not designed properly for 50 Ohms.

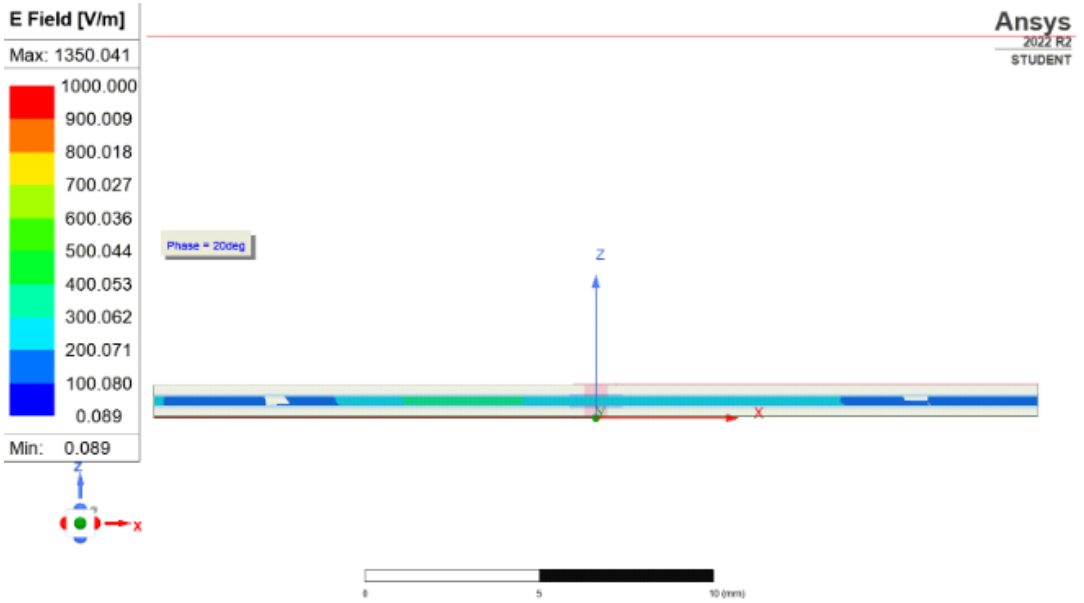

Figure 4: Cavity Noise - No Return Via Setup

B. 4 Return Via

This is the cavity noise observed when 4 return vias are present. As you can see there is a significant reduction in the amount of cavity noise present because of the return vias being present close to the transitioning via and also symmetrically.

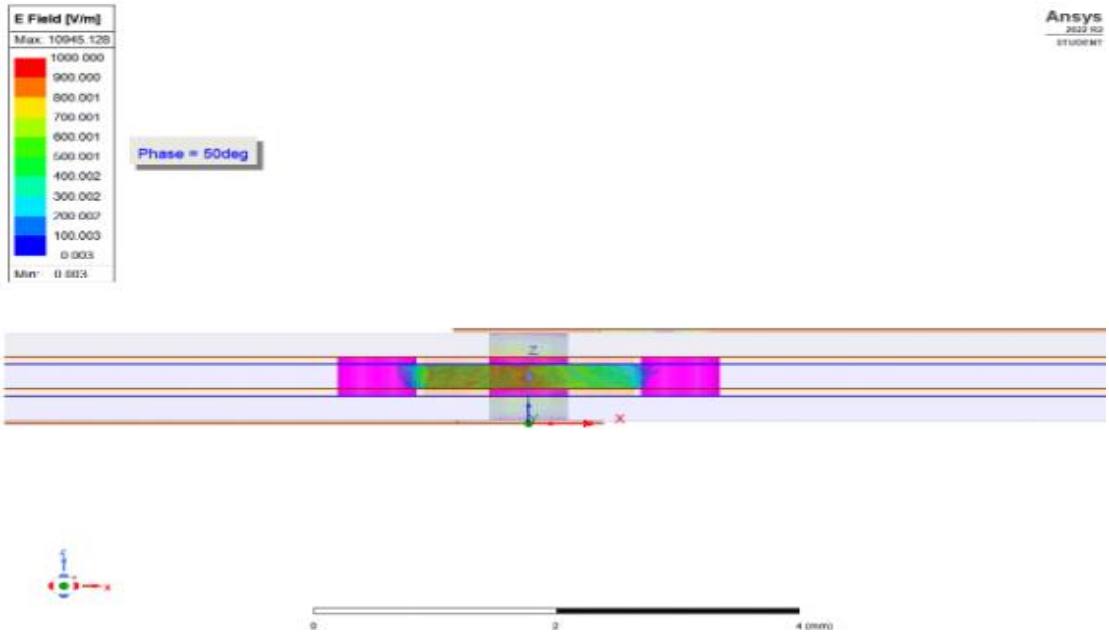

Figure 5: Cavity Noise - 4 Return Via Setup

C. S-Parameters

S-parameters, also known as scattering parameters, are a set of parameters that describe the behaviour of an interconnect that is under test [6]. They describe the relationship between the voltage and current at various points in the network. Insertion loss is a measure of the amount of signal power lost as a signal passes through a network, and it is defined as the ratio of the power entering the network to the power leaving the network [6]. Return loss, on the other hand, is a measure of the amount of signal power that is reflected back to the source due to a mismatch in impedance between the source and the network, and it is defined as the ratio of the power of the reflected signal to the power of the incident signal [6]. In S-parameter notation, insertion loss is represented by S21, while return loss is represented by S11.

S-parameter(return loss and insertion loss) were plotted on HFSS as shown by Figure 6. Observing the graph, we see for 1-via close to signal via, we see the S11 having sharp valleys (Red Output) as the frequency increase. We also observe S21 having small valleys as frequency increases (Green Output).

For the 4-via setup, here the return current has multiple paths to travel to the low impedance plane. Return loss S11 gets better (Blue output). S11 doesn't have any sharp valleys compared to S11 of 1-via. Insertion loss S21 improves and drops just a little (Orange Output) as frequency increases.

The signature of return and insertion loss shows how much loss your system inherits. Return loss (S11) is supposed to be a large negative value and Insertion loss (S21) is the amount of signal that gets to the receiver end. If S21 is 0dB it means the signal is transferred completely on the receiver end without any loss.

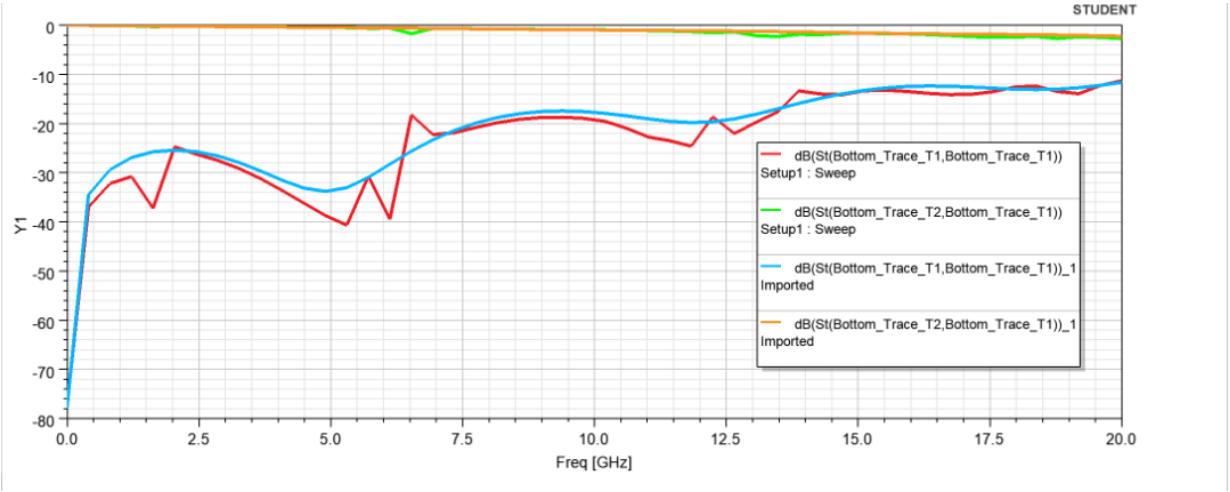

Figure 6: S-Parameter Output for 1- Return Via and 4 Return Via Setup

V. SYSTEM VALIDATION PART 2 - SIMULATION AND OBSERVATION

Designing a transparent via is challenging but quite important. When we have a 50 Ohms impedance trace that is designed as a controlled impedance line. When this trace transitions from one plane to another, it uses via. Via radius can change the impedance as per its design. It can either be inductive or capacitive. When the impedance increases, the via is inductive and when it decreases it is capacitive [8].

Keeping this in mind, we have to design the via such that it looks transparent when the signal changes layers. Here, we have designed the via close to transparent so that when the signal transitions, there are no reflections or a small number of reflections that get injected into the cavity. Noise in the cavity is the root cause of many problems that arise due to higher density designs. Noise in the cavity is due to the frequency components of return currents and the impedance of the cavity.

This noise results in crosstalk and ground bounce and can be pathological for your product.

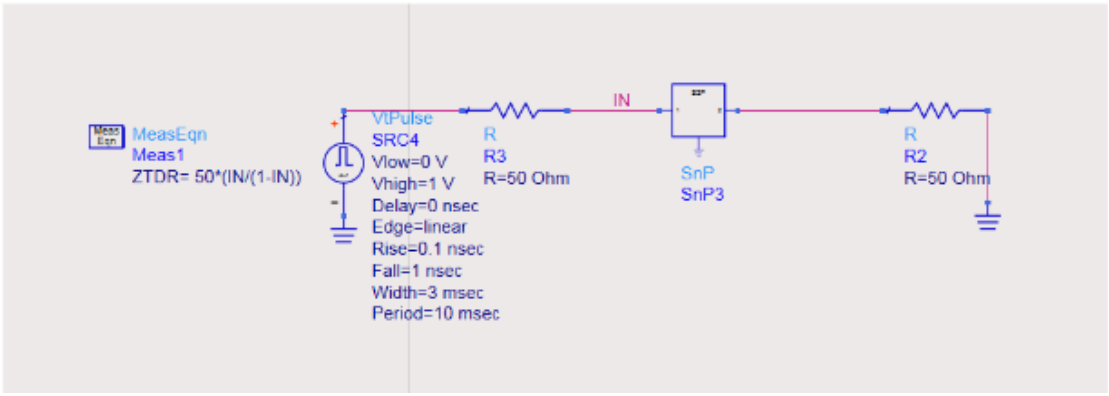

Figure 7: ADS Via Simulation Setup for TDR Measurement

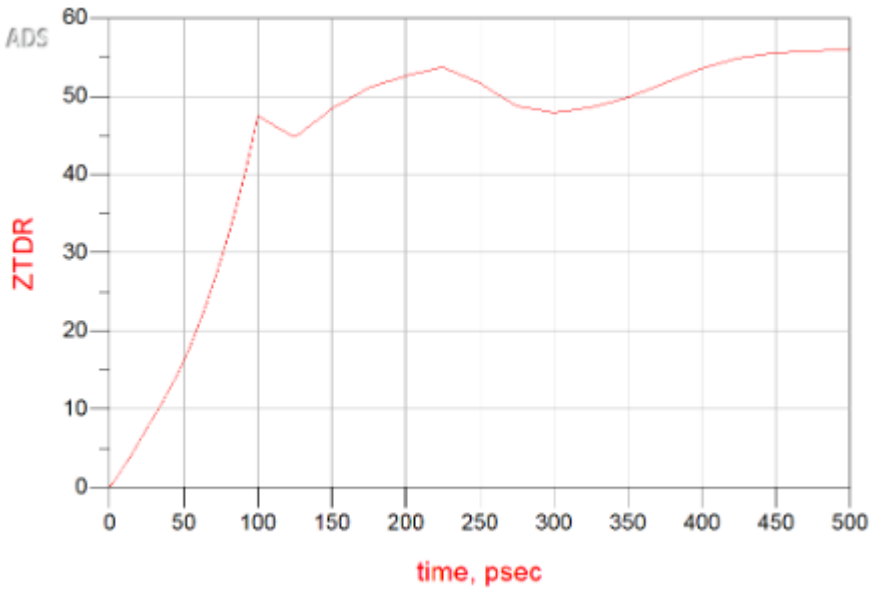

Figure 8: TDR Response of the Designed Via

VI. MITIGATION TECHNIQUES AND TERMINOLOGIES

Adding vias is one of the techniques used to mitigate the effects of signal transitions between layers in a 4-layer PCB with a stack-up of S-G-G-S. When a signal trace transitions between layers, it encounters a change in impedance [6][8], which can cause reflections, crosstalk, delay, and noise. Vias can help reduce the impedance mismatch by providing a low-impedance path between the signal trace and the ground plane.

Here are terminologies that might be helpful:

1) **Reflections**: When a signal transitions between layers, it encounters a change in impedance, which can cause reflections[8]. Adding vias to connect the signal layers to the ground planes can reduce the impedance mismatch, and hence, reflections.

2) **Crosstalk**: Crosstalk is the unwanted coupling of a signal from one trace to another trace[3]. When a signal transitions between layers, it can couple with other signals on the adjacent layer, causing crosstalk. By placing vias between the signal and adjacent planes, the coupling between adjacent signals can be minimized.

3) **Delay**: When a signal transitions between layers, it can experience a delay due to the change in the propagation speed of the signal [6]. By adding vias to provide a lowimpedance path between the signal trace and the ground plane, the delay can be minimized.

4) **Noise**: When a signal transitions between layers, it can pick up noise from the adjacent layer due to the coupling of electromagnetic fields[3]. By adding vias to connect the signal layer to the ground plane, the noise coupling can be reduced.

It is important to note that the effectiveness of vias in mitigating these effects depends on the size, placement, and number of vias used. Too few vias or improperly placed vias may not provide the desired benefits, while too many vias may result in increased capacitance and coupling between adjacent vias.

- **Always use Vss (ground) as the return plane:**

This statement suggests that the ground plane should always be used as the return path for signal traces. This is because the ground plane provides a low impedance path for the signal return current, which helps to minimize signal noise and interference.

- **Place at least one return via adjacent to every signal via:**

This statement suggests that a return via should be placed adjacent to every signal via to ensure a low impedance return path for the signal current. This helps to minimize signal noise and interference and improves signal integrity.

- **Use differential signals for all high-speed signals, minimize common signal component (mode conversion):**

This statement suggests that differential signaling should be used for all high-speed signals to minimize commonmode noise and mode conversion. Common-mode noise occurs when noise sources affect both signal traces in a differential pair, while mode conversion occurs when a differential signal converts to a common-mode signal due to impedance mismatches or other factors.

- **Still add return vias to reduce ground bounce from common signals:**

This statement suggests that return vias should be used even for common signals to reduce ground bounce. A ground bounce occurs when the ground voltage fluctuates due to the switching of the signal, which can cause noise and interference.

- **When return planes are not the same voltage, use return vias between similar planes: Vcc to Vcc and Vdd to Vdd:**

This statement suggests that return vias should be used between similar voltage planes (such as Vcc to Vcc and Vdd to Vdd) when the return planes are not at the same voltage. This helps to maintain a lowimpedance return path for the signal current.

- **When none of the return planes are the same, redesign the stack-up:**

This statement suggests that if none of the return planes is at the same voltage, the stack-up of the PCB should be re-designed to avoid potential signal integrity issues.

- **As a fallback, use as thin a dielectric as possible between different voltage planes and add low L decoupling capacitors between them:**

This statement suggests that if re-designing the stack-up is not possible, a thin dielectric should be used between different voltage planes to minimize the impedance mismatch. Additionally, lowinductance decoupling capacitors should be added between the voltage planes to provide a low-impedance path for the return current.

In summary, these statements suggest several mitigation methods for transitioning between layers using a via. By properly designing the size, placement, and number of vias, the impedance mismatch can be minimized, leading to better performance and reliability of the circuit. By following these guidelines, signal integrity can be improved, and potential noise and interference issues can be minimized.

VII. CONCLUSION

In conclusion, this paper investigated the effects of adding vias to a 4-layer PCB with a stack-up of signal-ground-groundsignal to mitigate the effects of signal transitions between layers. The study focused on the impact of vias on cavity noise, which is the noise generated due to the resonance of the cavity formed by the signal and ground planes.

The simulations conducted in this study showed that adding return vias around the via can significantly reduce the cavity noise compared to no return vias. Specifically, placing 4 return vias symmetrically around the via can reduce the cavity

noise by up to 40 dB compared to no return vias. Additionally, placing a return via close to the via can further reduce the cavity noise by up to 5 dB compared to 4 return vias symmetrically placed.

The results suggest that adding vias, particularly return vias, can effectively mitigate the effects of signal transitions between layers and reduce cavity noise. The study also highlights the importance of properly designing the size, placement, and number of vias to achieve optimal performance and reliability.

In summary, this study provides valuable insights into the design and optimization of PCBs with vias to improve signal integrity and minimize noise. The findings can be useful for engineers and designers working on high-speed PCBs and other electronic devices.

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