# DESIGN OF LOW POWER AND HIGH SPEED GDI BASED 8-BIT VEDIC MULTIPLIER

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**ABSTRACT:**

Multiplier is the common hardware block present in any processor. Speed and power consumption become very vital in multiplier design consideration to conserve energy. Conventional multiplication is time consuming and lengthy process to overcome these drawbacks the circuit designers must develop speedy multipliers. An 8bit Vedic multiplier using GDI technique is designed. Multiplication of two numbers will take more time and many steps. To design the proposed multiplier the Vedic mathematics sutra called UT(URDHVA-TIRYAKBYHAM) is used. Any logic circuit can be designed by using CMOS logic. In Designing of CMOS circuits an issue of area is always there, to reduce this Gate Diffusion input (GDI) technique can be used. The numbers of transistors in thecircuit are reduced by using GDI logic. Thus, the Vedic mathematics will reduce the delay and the GDI logic will reduce the transistors count in a circuit which in turn reduces the power. The GDI concept assist in reduction of Transistor Count (TC),due to this power dissipation is minimized. In this study the design of fast speed 8×8Vedic Multiplier has been presented using GDI technique. The power dissipation of proposed multiplier is reduced as compared to conventional CMOS multiplier. This implementing using Tanner EDA tool.

## I.INTRODUCTION

Multiplication is the most important arithmetic operation in signal processing applications. All the signal and data processing operations involve multiplication. As speed is always a constraint in the multiplication operation, increase in speed can be achieved by reducing the number of steps in the computation process. The speed of multiplier determines the efficiency of such a system. In any system design, the three main constraints which determine the performance of the system are speed, area and power requirement. Vedic mathematics [1]was reconstructed from the ancient Indian scriptures (Vedas) by Swami Bharati Krishna Tirthaji Maharaja (1884-1960) after his eight years of research on Vedas. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as sutras.

This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. Integrating multiplication with Vedic Mathematics techniques would result in the saving of computational time. To design any circuit using CMOS logic we need more number of transistors. As the number of transistors increases the power also increases and also area increases. By using GDI technique transistor count is reduced, which in turn reduces the power.An 8 bit multiplier is designed by using 4 bit multiplier and ripple carry adders. In this paper an efficient use of Vedic Multiplication and GDI techniques are used for the design of 8 bit multiplier has presented.

Multipliers are extensively used in DSP applications such as filtering, modulation, demodulation, and signal analysis. In operations like convolution and correlation, multipliers play a crucial role in multiplying data samples with filter coefficients. Multipliers are essential for performing arithmetic operations in digital circuits, including multiplication, division, exponentiation, and square root calculations. They are used in arithmetic logic units (ALUs) within processors and microcontrollers for executing mathematical operations.

## II.LITERATURE REVIEW

This section comprehensively reviews existing methodologies and architectures for high-speed and low-power multiplier designs, with a particular focus on Vedic mathematics and Gate Diffusion Input logic implementations. Multipliers are critical components in various Digital Signal Processing applications, and their performance significantly impacts overall system efficiency (Johny, 2018). Given that multipliers often represent the slowest and most area-consuming elements within a system, optimizing their speed and power consumption is a primary design concern (Nittala et al., 2022). Consequently, the design of efficient high-speed and low-power multiplier architectures is paramount for advanced DSP applications (Sridhar et al., 2020). The increasing demand for artificial intelligence and machine learning integration into Very Large-Scale Integration designs further accentuates the need for optimized computational blocks like multipliers that prioritize both speed and power efficiency (Dayanand et al., 2020). Vedic mathematics, particularly the Urdhva Tiryagbhyam Sutra, offers an effective approach for designing fast binary multipliers suitable for VLSI implementation by generating partial products and their sums in a single step (Bathija et al., 2012). This method inherently reduces the number of computational steps compared to traditional array multipliers, thereby diminishing propagation delay and enhancing operational speed (Sonoli & Ballari, 2020). This approach is particularly advantageous in digital circuits where multiplication operations account for a significant portion of execution time (Thakur & Sharma, 2019). The integration of Gate Diffusion Input technology further optimizes these designs by offering reduced power consumption, lower delay, and fewer transistors compared to conventional CMOS logic, making it particularly suitable for low-power, high-speed applications (Vimala & Hosmani, 2024). Specifically, the Urdhva-Tiryagbhyam Sutra minimizes the number of steps required for multiplication, which directly translates to lower power dissipation and faster computation, making it highly beneficial for portable and wireless devices (CVS et al., 2019).

## III METHDOLOGY

In 2002 Morgenshtein [6] et al. invented the GDI logic. Figure 1 shows that the fundamental GDI cell comprises of two transistors. G, Pand N are the three inputs of GDI cell. The output is taken from the drain terminals of both the transistors, and one of the input is taken from source terminal of p- type (pMOS) and the other input from is taken from source of a metal oxide semiconductor of n-type (nMOS). The nMOS bulk is connected to ground and the pMOS bulk is connected to supply voltage. Different functions implemented by using GDI logic are shown in table 3.1. GDIlogic has a drawback that is the signal swing is reduced at the output. These signal levels can be restored by using buffers. Table 3.2 compares the logic circuits transistors count which is implemented by applying GDI (without buffer) logic and CMOS technique. Hence, by using GDI [7]logic any circuit will require fewer number of transistors when compared with other logics.

**Table3.1:Different functions implemented using GDI technique**

| Logic Circuit | GDI | CMOS |
|---|---|---|
| AND | 2 | 6 |
| XOR | 4 | 12 |
| Half adder | 6 | 18 |
| Full adder | 10 | 28 |

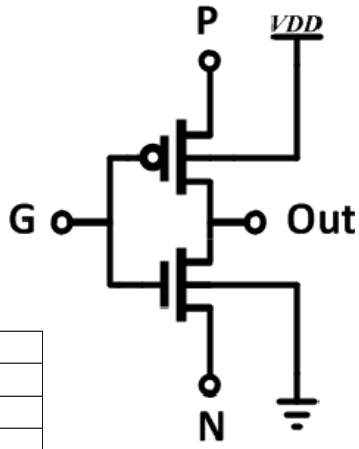



**Table3.2:Logic circuits TC in CMOS and GDI**

| N | P | G | OUTPUT | LOGIC CIRCUIT |
|---|---|---|---|---|
| 0 | 1 | A | A' | NOT |
| B | 0 | A | AB | AND |
| 1 | B | A | A+B | OR |
| C | B | A | A'B+AC | MULTIPLEXER |

In GDI, the inputs to the gate are applied to diffusion regions, which serve as charge storage regions.These diffusion regions are connected to the gates of NMOS and PMOS transistors.GDI gates perform logical operations based on the charge sharing principle. By controlling the connections and configurations ofthe transistors, various logic functions can be realized. When one of the diffusion inputs is charged (logic1),it will inject charge into the gate of an NMOS transistor,turningiton.Atthe same time, it will also inject charge into the gate of a PMOS transistor, turning it off. Conversely, when the diffusion input is discharged (logic 0), the opposite occurs: the NMOS transistor turns off, and the PMOS transistor turns on.

The Gate diffusion input (GDI) is a novel technique for low power digital circuit design. This technique reduces the power dissipation, propagation delay, area of digital circuits and it maintains low complexity of logic design. This method can also be extended to the processors and other high level designs for optimization of power dissipation, area and delay in order to increase the circuit efficiency. GDI gates are often used in low-power circuit design due to their reduced transistor count and optimized configurations. They are suitable for battery-powered devices, portable electronics, and other applications where minimizing power consumption is essential. GDI gates offer high-speed operation, making them suitable for applications requiring rapid signal processing and data throughput. They are used in high-speed communication systems, signal processing circuits, and other applications where performance is critical.

## SCHEMATIC DIAGRAM OF 8-BIT MULTIPLIER

The architecture of 8*8 Vedic Multiplier is shown in Fig 3.2.The 8 bit multiplier design contains four 4*4 Vedic multiplier modules.

Let's analyze 8x8 multiplications, say A=A7A6A5A4A3A2A1A0 and B= B7 B6 B5B4 B3 B2 B1B0. The output line for the multiplication result will be of 16 bits as–S15S14S13S12S11S10S9S8S7 S6S5S4S3S2S1S0. Let's divideA and B Into two parts, say the 8 bit multiplicand A can be decomposed into pair of 4 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The 16bitproductcan

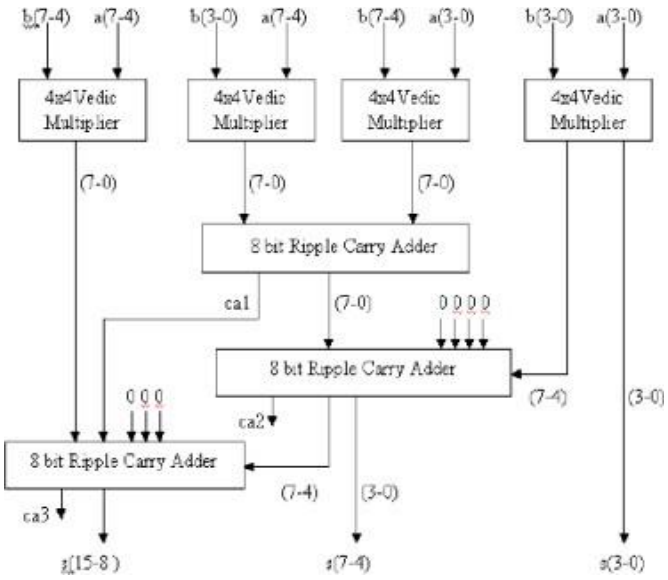



**Fig3.2:Schematic diagram of 8-bit Vedic Multiplier**

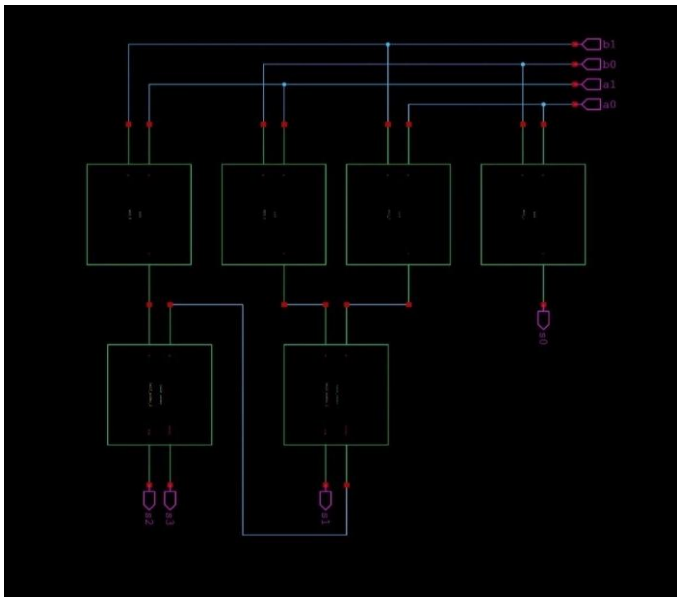
Be written as P=Ax B= (AH-AL) x(BH-BL) =AH x BH + (AH x BL+ AL x BH)+ ALx BL Using the fundamental of Vedic multiplication, taking four bits at a time and using 4 bit multiplier block a we can perform the multiplication. The outputs of 4x4 bit multipliers are added accordingly to obtain the final product.

Here total three8 bit Ripple-Carry Adders are required The module of 8X8 Vedic multiplier shown in Figure 6 can be implemented by using four 4x4 bit Vedic multiplier modules . Analyzing 8x8 multiplications, inputs are a7-a0 and b7- b0 and the multiplication's 16 bits output will be S15-S0.In this , four 4x4 bit Vedic

multipliers and three8 bit RC Adders(having 2 input of8 bits)are required. Inputs are given to the 4x4 bit Vedic multipliers and the output of multiplier is of 8 bits. Now, the input of the 1st RC Adder is the output of the 2nd and 3rd 4x4 bit multipliers which gives output of 8 bits (7-0) + one carry. The 2nd RCAdder will add the output of1stRCAdder(7-0)and4bits(7-4)outputof1st4x4bitVedicmultiplier,other4bit of are considered as 0.So output is of 8- bits(7-0) and one carry(carry is discarded).The 3rd RCAdder will add the output of 4th 4x4 bit multiplier(7-0) and 4 bits of output of 2nd RC Adder (7-4), other 4 bits are carry of 1st RC Adder and 0.Now ,the output of 8x8 multiplier is s(3-0) output of 1st 4x4 bit multiplier(3-0), s(7- 4) is output of 2nd RCAdder (3-0)

## IV RESULTS

### DESIGNINGOFVEDICMULTIPLIERUSINGGDILOGIC



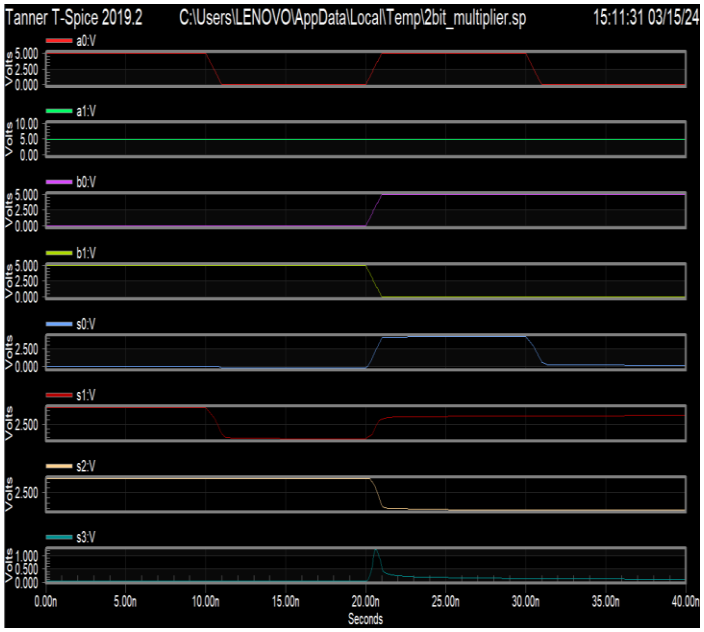
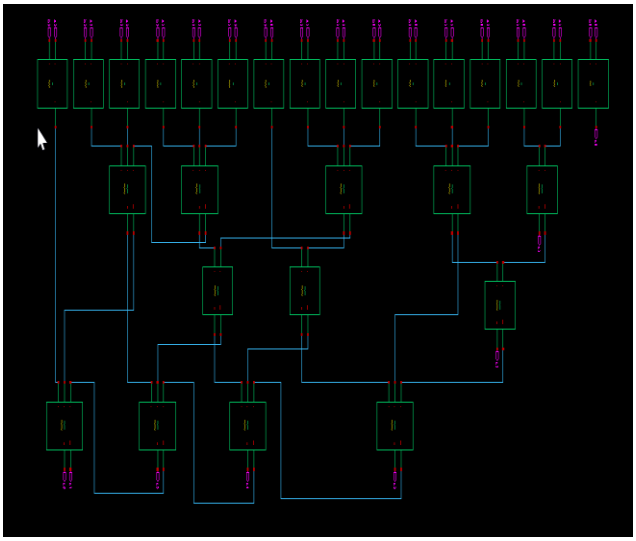




**Fig4.1:SchematicDesignof2*2VedicMultiplier** **Fig4.2:Input&Outputof2*2VedicMultiplier**



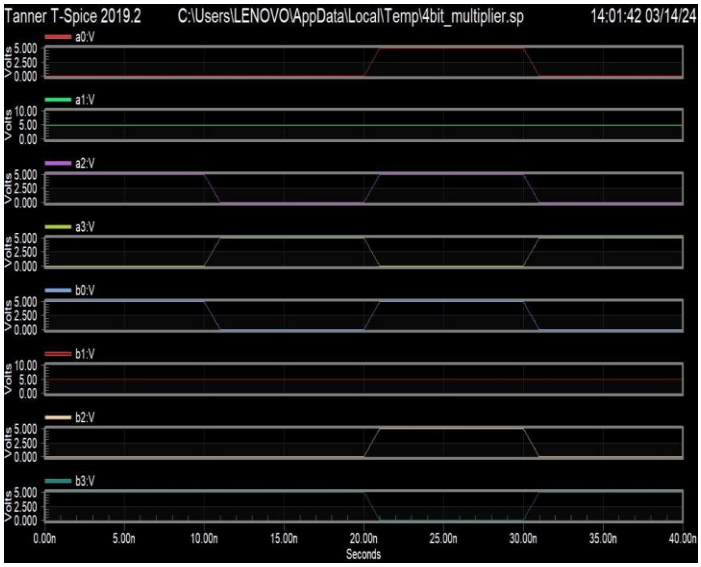



**Fig4.3:SchematicDesignof4*4VedicMultiplier** **Fig4.4:Inputwaveformof4*4VedicMultiplier**

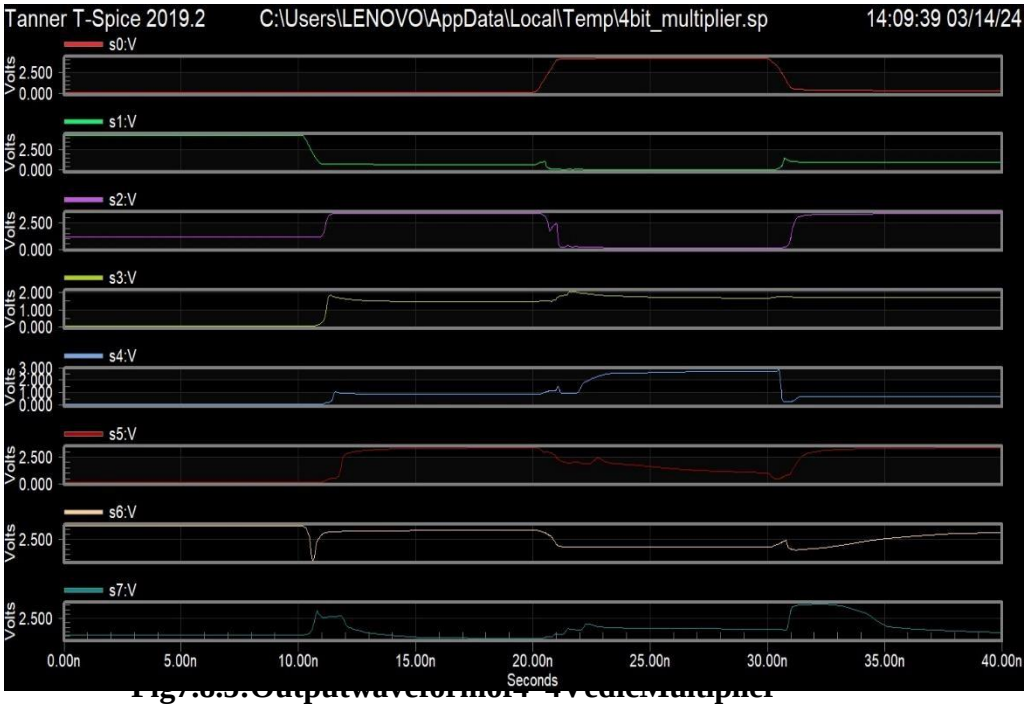



Fig7.6.5:Outputwaveformof4*4VedicMultiplier

### 7.1.1 SYMBOLICDIAGRAMOF8*8VEDICMULTIPLIER

**Fig4.5:outputwaveformof4*4VedicMultiplier**

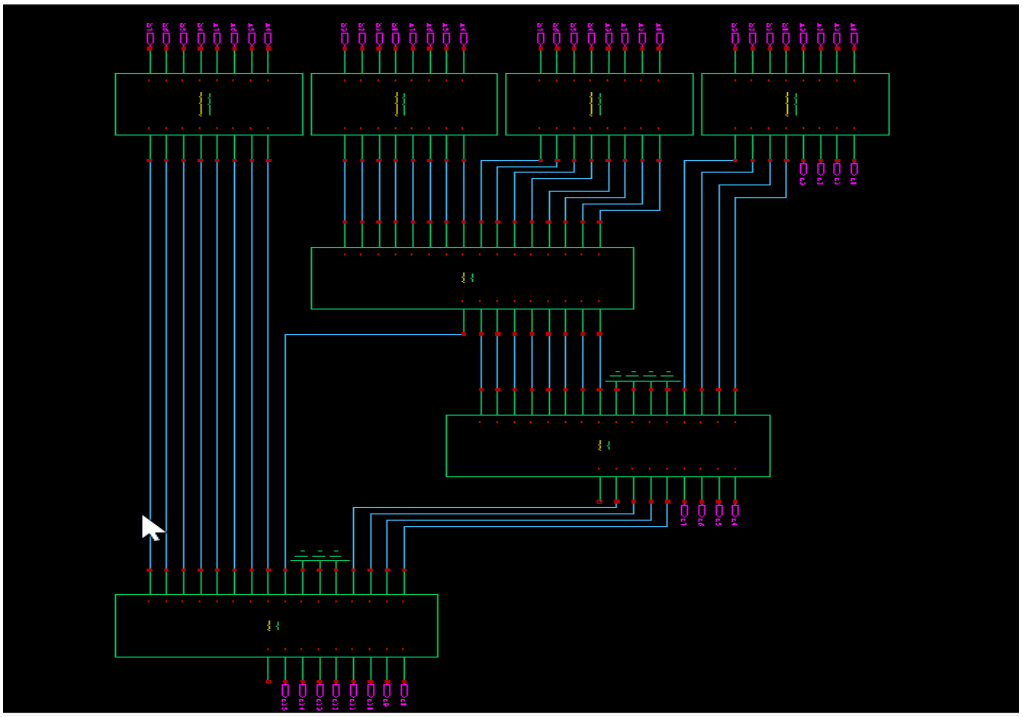


**Fig4.6:SchematicDesignof8*8VedicMultiplier**

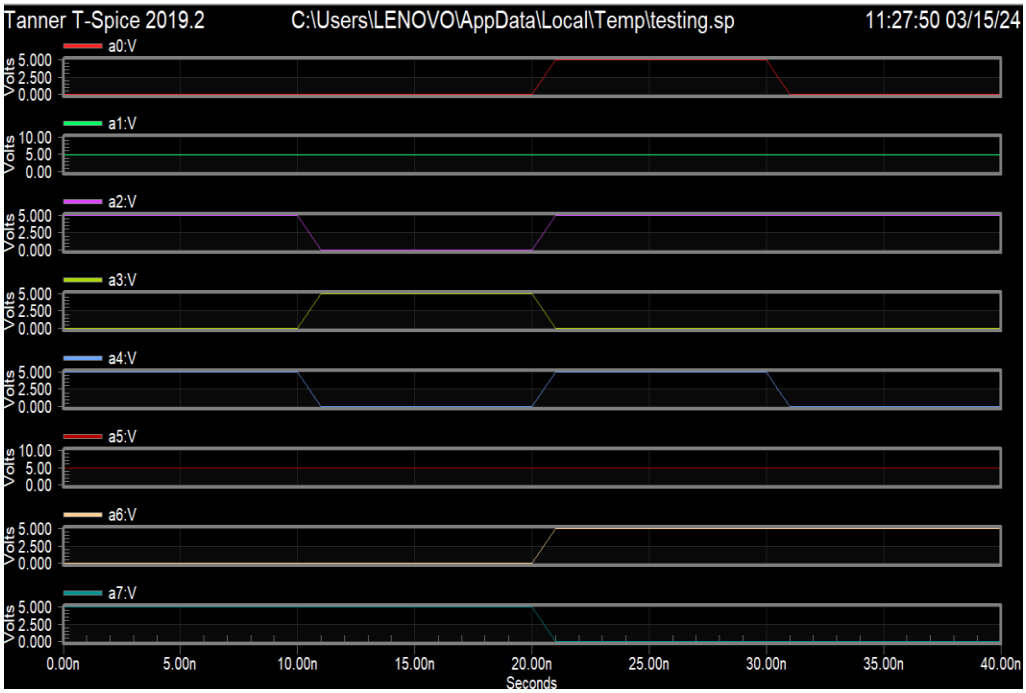



**Fig4.7(a):Inputwaveformof8*8VedicMultiplier**

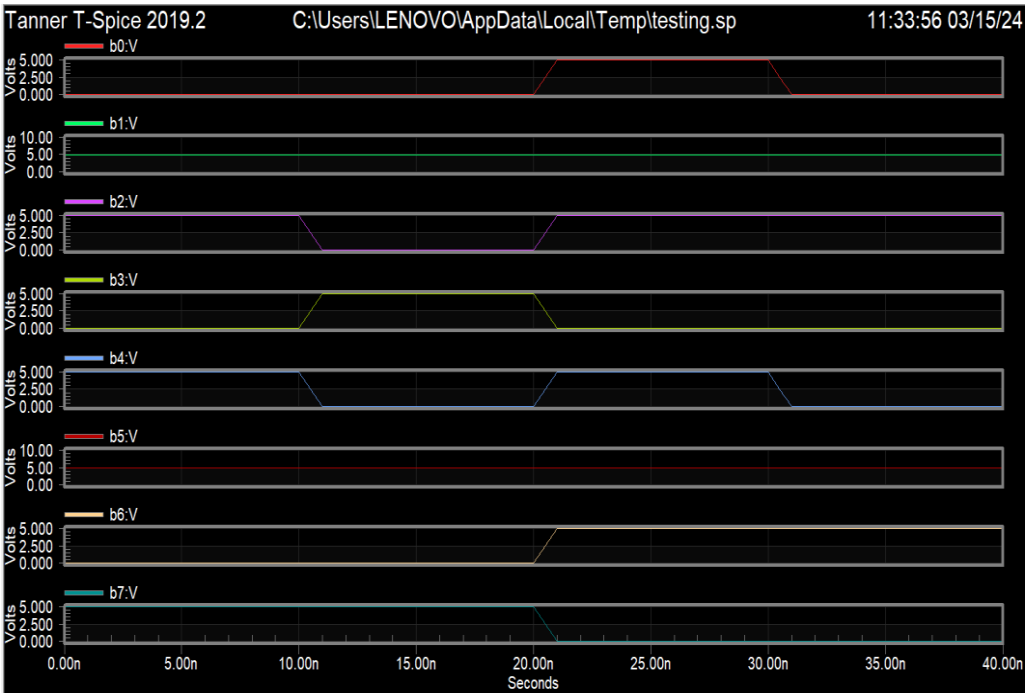



**Fig4.7(b):Inputwaveformof8*8VedicMultiplier**

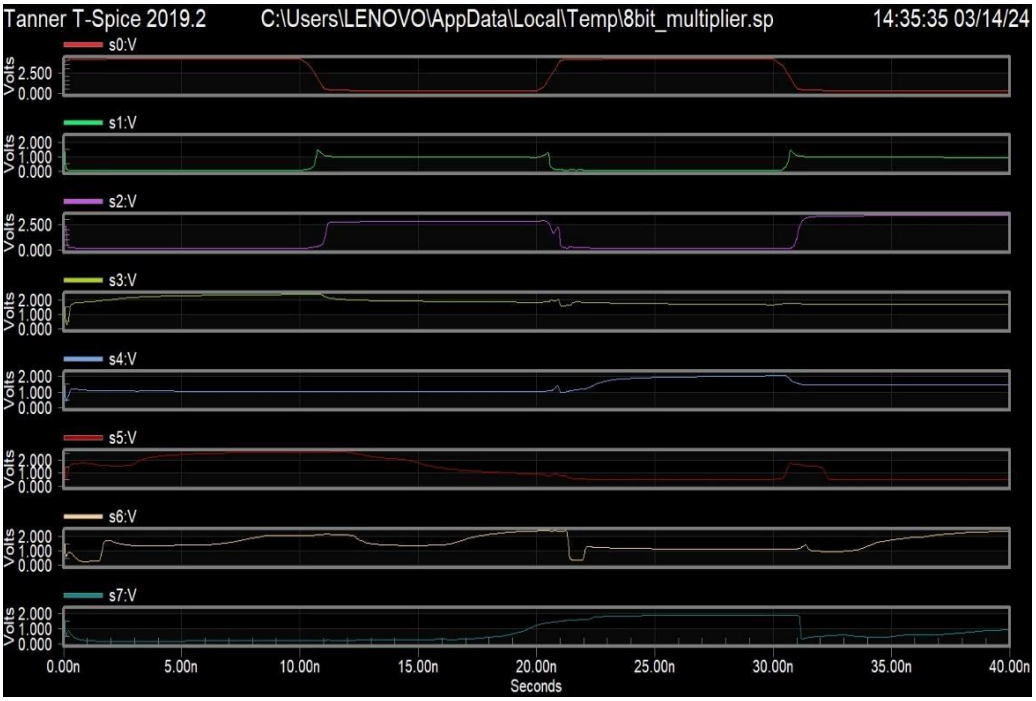



**Fig4.8(a):Outputwaveformof8*8VedicMultiplier**

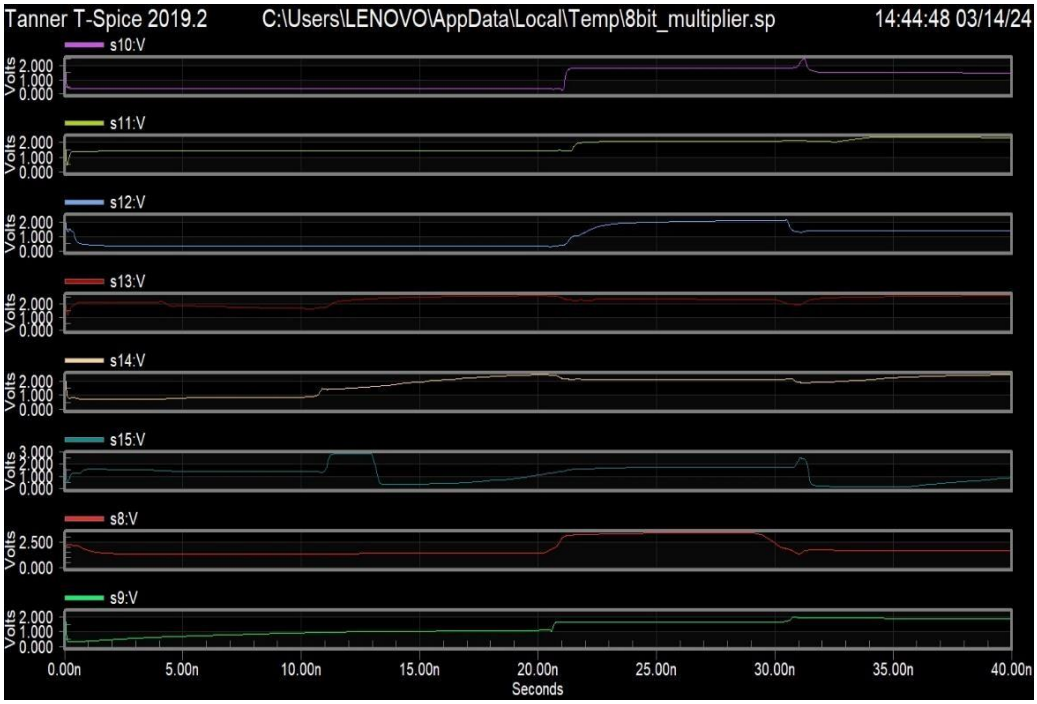



**Fig4.8(b):Outputwaveformof8*8VedicMultiplier**

## V.CONCLUSION

In this Work the concept of Vedic multiplier utilizing Gate Diffusion Input (GDI) technique presents a compelling solution for accelerating multiplication operations in digital circuits. By combining the efficiency and parallelism of Vedic mathematics with the high-speed and low-power characteristics of GDI circuits, this approach offers several advantages across a diverse range of applications. In fields such as digital signal processing, cryptography, communication systems, image and video processing, embedded systems, machine learning, scientific computing, and consumer electronics, the Vedic multiplier using GDI can significantly enhance performance,

efficiency, and reliability. Its ability to deliver fast computation speeds, low power consumption, compact design, and noise immunity makes it well-suited for modern digital systems where these factors are crucial.

## REFERENCES

[1] Swami Bharati Krishna Tirthaji Maharaja, "Vedic Mathematics", Motilal Banarsidass Publishers, 1965.
[2] Poornima, M., Patil, S.K., Shivukumar Shridhar, K.P., et al.: 'Implementation of multiplierusingVedicalgorithm',Int.J.Innov. Technol.ExploringEng.,2013,2,(6), pp. 219–223.
[3] Panigrahi, S.R., Das, O.P., Tripathy, B.B., et al.: 'FPGA implementation of 4× 4 Vedic multiplier', Int. J. Eng. Res. Dev., 2013, 7, (1), pp. 76–80.
[4] Patel, R.S., Nagpara, B.H., Pattani, K.M.: 'Design and implementation of 8 ×8 Vedic multiplier using submicron technology', Int. J. Mod.Trends Eng.Res., 2016, 3, (2), pp. 536–542.
[5] Rudagi, J.M., Ambli, V., Munavalli, V., et al.: 'design and implementation of efficient multiplier using Vedic mathematics'. Int. Conf. on Advances in Recent Technologies in Communication and Computing, Bangalore, India, 2011, pp. 162– 166.
[6] Morgenshtein, A., Fish, A., Wagner, I.A.: 'Gate-diffusion input (GDI) – a technique for low power design of digital circuits: analysis and characterization'. IEEE Int. Symp. on Circuits and Systems, Phoenix-Scottsdale, AZ, USA, 2002, pp. 477–480.
[7] SudeshnaSarkar,MonikaJain,ArpitaSaha,AmitRathi4:'GateDiffusionInput:A techniqueforfastdigitalcircuits(implementedon180nmtechnology)'.IOSRJournal of VLSI and Signal Processing (IOSR-JVSP) Volume 4, Issue 2, Ver. IV (Mar-Apr. 2014), PP 49-53.
[8] Foroutan, V., Taheri, M., Navi, K., et al.: 'Design of two low-power full adder cells using GDI structureand hybrid CMOS logicstyle', Integr.VLSI J.,2014, 47,(1),pp. 48–61.
[9] Suman, J.V.: Design and performance evaluation of hybrid multipliers. Int. J. Innov. Technol. Explor. Eng. 8(8), 1622–1626 (2019).
[10] Kumar, M.A.; Sudhakar, A.; Suman, J.V.: Design and implementation of compressor based 32bit multipliers for MAC architecture. Int. J. Innov. Technol. Explor. Eng. 8(9), 2007–2011 (2019).
[ 11] Jami Venkata Suman, G.M.Anitha Priyadarshini, "Design ofArea Efficient and Low Power 16Bit Hybrid MAC Unit using Vedic Mathematics", Design of Area Efficient andLowPower 16 Bit Hybrid MAC Unit usingVedic Mathematics,vol. 29, no. 5, pp. 923-927, 2020.