A HYBRID FULL ADDER USING A NOVAL XOR GATE FOR LOW POWER APPLICATION

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***Abstract*- Using a combination of Pass Transistor Logic (PTL), CMOS logic, and transmission gate (TG) logic in 65-nm technology, a unique Hybrid Full Adder (HFA) has been developed. This implementation includes various modules such as the XOR module, the carry generator module, and the sum generator module, which are used to realize a 1-bit HFA. To design the proposed HFA, an inverter logic is used in conjunction with the XOR logic to obtain the logic of XNOR. The proposed design is impressive as it uses only 13 transistors, resulting in a small area. This improvement in terms of Power-Delay Product (PDP) makes it suitable for basic building blocks of Very Large-Scale Integration (VLSI) circuits. Furthermore, the power consumption of the proposed HFA is significantly lower, resulting in improved PDP compared to other hybrid full adders. A comparison of the essential parameters between the proposed HFA and other existing HFAs has been made.**

Key Words: **Hybrid full added, XOR Gate, XNOR gate,**

INTRODUCTION

The increasing demand for battery-powered electronic devices like the Personal computer, smart phones, bioelectronics and PDA devices. Very Largescale Integration (VLSI) designers are focused towards minimum power delay characteristics of the circuits . One of the major concern for designers to achieve minimum power delay is to design energy efficient VLSI circuit . In order to develop a low power VLSI circuit, the designer need to consider the transistors count, heat transfer and area of the circuit. The main goal is to keep the battery life longer with reduced cost and area of packaging which is suitable for portable device applications So, researchers are developing efficient basic circuits for the application of low- power circuits by implementing hybrid technology. As a result, the performance microelectronic circuits is improved in a tremendous manner. A one bit Full Adder (FA) is considered as a basic logic module of building arithmetic logic circuits like binary addition, subtraction and multiplier etc. Hence, highly efficient basic FA blocks in the arithmetic logic unit (ALU) circuit is needed for large scale arithmetic operation of high resolution image and video processing, and many other microprocessor applications. The complementary metal-oxide semiconductor (CMOS), Transmission gate FA and dynamic CMOS logic are the most widely used logic styles for the building of 1-bitFA. The conventional CMOS logic style is widely preferred due to its excellent driving capabilities and good output swing. But, the drawback of employing CMOS circuits is its higher power consumption due to high current switching time and leakage of current due to short circuit. Further, the design can be implemented by using multiple logic which are known as hybrid logic, to enhance the overall performance of the FA. Hybrid logic styles consist of two or more different logic styles CMOS-CPL, PTL-TGA, CMOS-TG, hybrid CMOS, for designing the circuits. Arithmetic operation such as additions and subtraction and also in multiplication and division are widely used and play an important role in various digital systems such as digital signal processor (DSP) architecture and also for microprocessor further being used in microcontrollers and data process unit. Although adders are the logic circuits that had being designed to perform some of the high speed arithmetic as well as logical operations and are important components in digital system because of their extensive use in other basic operations such as subtraction and multiplication and good to be likely used for division Nowadays in many of computer and other kinds of processor and adders are likely to be used hence not only in the arithmetic logic unit functions but also in other important parts of the processors where they are used to calculate addresses and table indices and same kind of operations performed thus the very basic arithmetic operations is the adding of two binary digits bits. A conventional ALU can be used to perform basic arithmetic and logic operations such as AND, OR, NOT,ADD, Subtract. The Arithmetic logic unit take two operands and also performs the desired operations between those units also the control signal is to be used to select the output from the operations that had been performed thus; the control unit is designed by using a multiplexer which selects the required operations. All the operations are performed in one cycle but only the one that is required in the output is selected by the Multiplexer and an Arithmetic logic unit does not perform multiplication between two operands and also an extra circuitry is being required along with the Arithmetic logic unit which increase the chip area therefore, in this paper we propose the design of an ALU which supports multiplication. The Multiplier is designed using the Both's algorithm is a multiplication algorithm that multiplies two numbers which are binary by using two's complement notation also in an conventional array multiplier requires a large number of devices.

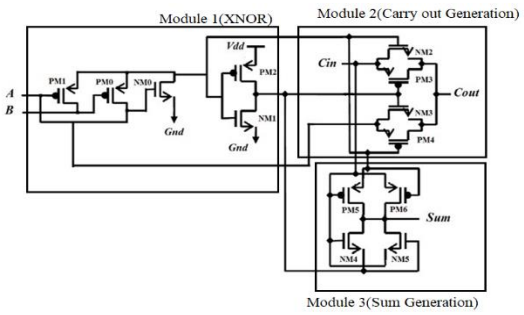
LITERATURE REVIEW

Salam Surjit Singh in November 2020 A unique 1-bit HFA is designed using a standard cadence virtuoso platform at 90-nm technology. The transistor count of the designed HFA is only 13T, which is less than the reported hybrid style. Moreover, the designed HFA has less power and power delay product compared to the existing FA design. The results of the proposed HFA have improved in overall performance in terms of power delay. The area of the circuit is significantly smaller because of 13 transistors used in the proposed HFA. In future, the layout of the designed HFA may be done to study the area of the proposed

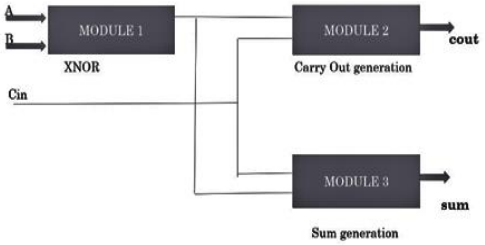
circuit. Further, a 1- bit HFA design can be implemented in designing a 32-bit HFA and 64-bit Ripple carry Adder in various nano meter technologies to study and improve the overall performance**. Keivan Navi and Omid Kavehei** in February 2008 presented new low power and high performance adder cell using a new design style called using Bridge design style ofthe MOS transistor. The bridge design style enjoys a high degree of regularity, higher density than conventional CMOS design style as well as lower power consumption, by using named bridge transistors. Their new design style uses some transistors, named bridge transistors, sharing transistors of different paths to generate new paths from supply lines to circuit outputs They presented the Simulation results by using 65nm technology based on the CMOS circuits. They used H-SPICE to verify the circuits and presented the superiority of the resulting of their proposed adder circuits against conventional CMOS 1-bit full-adder in terms of power and delay. They have done the characterization of theircircuits by varying the different voltages supply ranging from 0.65v to 1.5v with 0.05v steps. The main focus of their design work is basically on the power delay product and dynamic power dissipation also they have presented the improvement in the overall delayof the circuit. According to their simulation results on HSPICE EDA tool, 65 nm CMOSprocess technology at room temperature, and under given conditions, shows the improvements of 41.5%. At the lower voltages (0.65v) there is impressive improvementof the dynamic power dissipation is being presented but static power dissipation is no longer has been shown in this paper. **Ilham Hassoune and Denis Flandre** in 2010 presented a technique in adder to improve the noise margin and also reduction in the average power they basically use optimized level shifter at the output of the adder circuit and also they had used low powerXOR and XNOR circuits to optimize the whole adder circuits however they have shownthat their circuit also need complement and original input of the input signal which somewhat increases the area of the silicon chip. **Navi, Mohammad Hossein Moaiyeri, Reza Faghih Mirzaee**, Omid Hashemipour,Babak Mazloom Nezhad proposed a concept of "Two new low-power Full Adders basedon majority-not gates" Two novel low-power 1-bit Full Adder cells have been proposed. Both circuits use only two majority-not gates, which are implemented using new methods. The first design used only capacitors and CMOS inverter gates, while the second one hasbenefited from a high-performance CMOS bridge circuit, which has improved the parameters of the first design. Low power consumption has been targeted at the circuit design level for both cells.

PROPOSED METHOD

It shows the FA implementation which gives out Sum and Carry logics as output by giving A, B, and Cin as input signal. Module 2 and module 3 gives the finaloutput of the FA circuit which is implemented using XOR and XNOR logic there are 13t is used. The structure is given in figure 5.1 1-bit hybrid full adder



1.1 Circuit diagram of 1-bit hybrid full adder



1.2 Block Structure of Full Adder

PMOS AND ITS WORKING

A PMOS transistor is a type of MOSFET that utilizes a p-type semiconductor material as the channel, with source and drain terminals formed on the same material. The gate terminal is placed on an insulating layer of metal oxide. When a positive voltage is applied to the gate terminal, a depletion region forms in the p-type semiconductor material, effectively blocking current flow between the source and drain terminals. Lowering the voltage on the gate terminal causes the depletion region to disappear, allowing current to flow. PMOS transistors are typically normally-off devices since their channels are made of p-type material, which means they remain off when there is no voltage applied to the gate terminal and turn on when voltage is applied. They are commonly utilized as load devices in digital circuits and input devices in analog circuits. PMOS transistors possess advantages and disadvantages compared to other types of transistors. One of their advantages is that they have higher noise margins than NMOS devices, which makes them less prone to signal interference. Furthermore, they are efficient in low-power applications because they consume less power when in the off state. However, PMOS transistors have certain limitations. They generally have slower switching speeds than NMOS transistors, which makes them unsuitable for high-frequency applications. They also have lower carrier mobility, which limits their ability to handle as much current as other types of transistors. Despite these drawbacks, PMOS

transistors continue to be widely used in digital and analog circuits. Their high noise margins and low-power operation make them ideal for specific applications, such as voltage regulators and level shifters.

NMOS AND ITS WORKING

The NMOS transistor is a MOSFET that employs an n-type semiconductor material as the channel, with the source and drain terminals placed on the same material. The gate terminal is positioned on an insulating layer of metal oxide. The application of a positive voltage to the gate terminal generates a depletion region in the n-type semiconductor material, allowing current to flow between the source and drain terminals. The depletion region disappears when the voltage on the gate terminal is reduced, which blocks the flow of current. The NMOS transistor is typically a normally-on device, as its channels are made of n-type material, indicating that it remains on when no voltage is applied to the gate terminal and turns off when voltage is applied. NMOS transistors are commonly employed as switching devices in digital circuits and output devices in analog circuits. In comparison to other types of transistors, NMOS transistors have both advantages and disadvantages. One of their advantages is that they have fast switching speeds compared to PMOS devices, making them ideal for high-frequency applications. They also have higher carrier mobility, enabling them to handle more current than PMOS transistors. However, NMOS transistors also have some limitations. They have lower noise margins than PMOS devices, which makes them more vulnerable to signal interference. Additionally, they consume more power than PMOS transistors in the off state. Despite these limitations, NMOS transistors are widely used in both digital and analog circuits. Their high carrier mobility and fast switching speeds make them ideal for microprocessors and memory circuits.

XOR Module

The high power consumption of the XOR module within the adder circuit poses a significant challenge. A solution is required to develop an XOR module that consumes less power. In response to this challenge, an XOR module has been proposed for the HFA circuit with a focus on reducing power consumption. The proposed module accomplishes this by adjusting the length and width of transistors to obtain the desired output current. To minimize power consumption, the PMOS resistance (PM0) in the XOR module is reduced by adjusting its dimensions. Furthermore, the sizing of the final NMOS transistor in the module is optimized. Table I outlines the logic table for XOR. The new XOR module's design objective is to reduce power consumption while maintaining functionality. Through transistor dimension optimization, the proposed module successfully achieves this goal and can be effectively implemented in the HFA circuit. The XNOR (exclusive-NOR) operation is a logic operation that returns a TRUE value only if both its inputs are either TRUE or FALSE. In other words, it produces a TRUE output when both inputs have the same logic value, and a FALSE output when they have different logic values. The XNOR operation can be implemented using various digital logic gates, including the XNOR gate, the NAND gate, and the NOR gate. Each of these gates has its own unique set of characteristics and advantages, but they all perform the same basic function of implementing the XNOR operation. One of the simplest ways to understand the working of the XNOR operation is to consider its truth table.

CARRY AND SUM GENERATION MODULE

Sum

The output value produced by adding three input bits, A, B, and carry-in (Cin) in a full adder is referred to as the "sum". This operation generates a binary sum output (Sum) that represents the result of the addition. For example, if A=1, B=1, and Cin=0 are given as inputs to a full adder, the sum output (Sum) would be 0 with a carry-out (Cout) of 1. This is because the binary sum of 1 and 1 is 10, which is represented as 0 with a carry-out of 1.

Carry

The carry in (Cin) is an input bit in a full adder that represents the carry from the previous addition operation. During the current stage of the addition operation, the carry-in bit is added to the two binary digits, A and B. For instance, in adding two 4-bit binary numbers, the carry-in (Cin) for the first bit is 0, and for the subsequent bits, it is the carry-out (Cout) generated by the previous stage of addition. The carry-in bit is optional and can be set to 0 if there is no carry from the previous addition operation. The carry-out (Cout) generated by the current stage represents the most significant bit (MSB) of the addition result. In the proposed HFA circuit, the carry signal (Cin) is generated using TG logic, where the dimension of the PMOS and NMOS transistors used in TG is kept at 120 nm and 100 nm as length and width. The result of the weak inverter provides the XNOR logic, and the output of XNOR is applied between PM3 and NM3 transistors of the Cout block to complete the Cout module. Finally, the result of the XNOR logic is connected to NM4 and NM5 transistors to complete the SUM part. The proposed 1-bit HFA was simulated using 65-nm technology, and the block diagram showing the input and output representation of the designed HFA. The aim of this proposed HFA design is to reduce the power consumption of the FA circuit and increase its speed. As a result, the PDP of the proposed design is reduced. The proposed HFA is compared with other HFAs in the 65-nm process technology, where it used only 13 transistors, while existing HFAs used 16 transistors. The average power of the circuit is significantly lower than that of other reported hybrid FAs, and the speed of the HFA is also improved.

SOFTWARE/TOOL USED

Tanner EDA is a software tool that is used in the design and verification ofdigital circuits, specifically for the design of error correcting codes (ECC) such as low-density parity-check (LDPC) codes and turbo codes. It provides a comprehensive set of

tools for the design, simulation, and optimization of ECC circuits, including support forvarious code structures, various decoder architectures, and various channel models. Electronic Design Automation, or EDA, is a market segment consisting of software, hardware, and services with the collective goal of assisting in the definition, planning, design, implementation, verification, and subsequent manufacturing of semiconductor devices, or chips. Some of the features of Tanner EDA includes support for various code structures such as regular, irregular, proto graph-based and spatially coupled, various decoder architectures such as belief propagation, sum-product and min-sum, and various channel models like AWGN, BSC, BEC and Rayleigh fading. Tanner EDA also includes a variety of analysis and visualization tools that can beused to gain insight into the behavior of ECC circuits, such as bit error rate (BER) and frame error rate (FER) simulation, and constrain the design space. Additionally, it has support for Matlab and C++, which allows the users to integrate their own decoders and simulations. with its wide range of features and functionalities, it enables designers to quickly find the best design for their specific application and channel conditions, while also taking into account the constraints of thetarget device or system.

Advantage of Tanner EDA Tool

There are several advantages of using the Tanner EDA (Electronic Design Automation) tool:

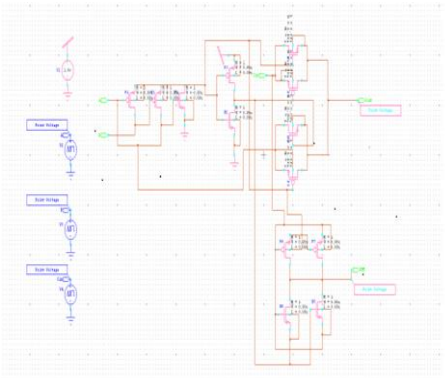
1. High-quality layout generation: Tanner EDA provides advanced layout generation capabilities, which result in high-quality layouts that meet design specifications.
2. Wide range of supported technologies: The tool supports a wide range of technologies,including CMOS, BICMOS, and bipolar technologies, making it suitable for a varietyof design projects.
3. Automated design flows: Tanner EDA includes automated design flows that can helpspeed up the design process and reduce the likelihood of errors.
4. Advanced verification capabilities: The tool includes advanced verification capabilities, such as DRC (Design Rule Checking) and LVS (Layout vs. Schematic),
5. Multi-language support: Tanner EDA supports a variety of languages, includingVerilog, VHDL, and SPICE, making it easy to integrate with other design tools and environments.

Easy-to-use interface: The tool has an intuitive and easy-to-use interface, which helpsto reduce the learning curve for new users.

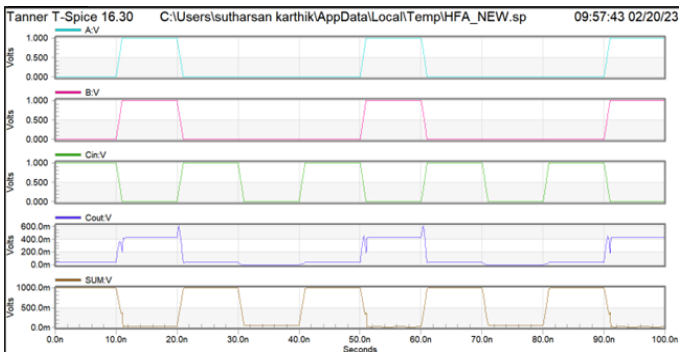
RESULT

A	B	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

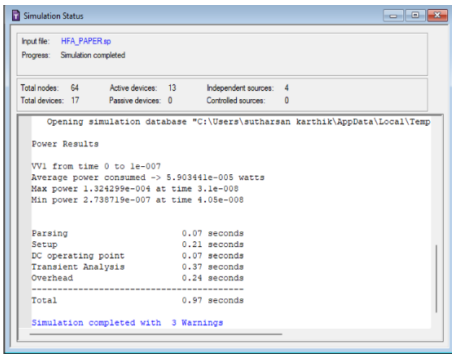
EXISTING METHOD



EXISTING WAVEFORM



EXISTING OUTPUT



COMPARATION OF 90nm AND 65nm TECHNOLOGY

S.NO	**90nm Technology**	**65nm Technology**
1	Average power consumed **=>1.775929**watts	Average power consumed **=>1.75724**watts
2	Transient Analysis 0.09 sec	Transient Analysis 0.08 sec
3	DC operating point 0.03 sec	DC operating point 0.03 sec
4	Overhead 0.95 sec	Overhead 0.12 sec
5	Power consumption is more high	Low power consumption

CONCLUSION

A HFA is developed using a standard CMOS process technology with a 65-nm node and only 13 transistors, which is less than the previously reported hybrid styles. Compared to existing FA designs, the proposed HFA exhibits improved performance with lower power consumption and power delay product. Furthermore, the circuit size is significantly reduced due to the small number of transistors used in the design. Future work may focus on layout optimization to further reduce the circuit area. The power consumption analysis reveals that the proposed HFA consumes less power than the 95nm technology, while the 65nm technology offers better performance with low power consumption. The proposed HFA also displays higher speed and power performance, with an average power consumption of 78.04µW. Overall, the designed HFA represents a significant advancement in terms of power and size, making it suitable for low-power VLSI applications.

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