DESIGN OF FULL ADDERS USING DOUBLE GATE MOSFET

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Abstract: The need of designing low power VLSI circuits has been increased immenselydue to increased demand of portable devices like Laptops, cellular and mobiles. Further to integrate a greater number of devices on chip, scaling of device size is required. But there are number of problems in scaling of bulk MOSFETS. The problems like leakage current, drain induced barrier lowering (DIBL) effect, and other short channel affects (SCE's) degrade the performance of circuits. New device structure is needed which can work with improved performance in nano- meter range of operation. A double gate MOSFET is capable device because it shows better scalability in nano circuit. Double Gate MOSFET (DG MOSFET) is widely used in ultra-low power design. This thesis explains the performance analysis of Single Gate and Double Gate MOSFET. This structure not only reduces the count of transistors by 86% but also demonstrates that larger circuits of double gate MOSFETs can be built, bolstering the faith in double gate MOSFET devices as a possible substitute of CMOS devices in a near future.

Keywords: Low Power VLSI, MOSFET (DG MOSFET), , Short Channel Effects (SCEs), Drain Induced Barrier Lowering (DIBL), Nano-scale Devices, CMOS Scaling, Ultra-low Power Design.

I INTRODUCTION

The power consumption and speed improvement are key goals in the design of digital processing units, especially for portable systems. Normally, an increase in speed is achieved at the cost of both power consumption and computation exactness. This approach, known as approximate computing, may be used for applications where some errors are tolerable. Digital Signal Processing (DSP) often handles human sense-related signals. Since human perceptual abilities are limited, approximate computing can be invoked for custom DSP blocks processing these signals. Adder blocks, the main components in arithmetic units of DSP systems, are power-hungry and often form hotspot locations on the die. These facts motivate realizing this component using approximate computing. Such adders improve delay and energy compared to state-of-the-art approximate adders and are less vulnerable to delay variation than conventional ones. As more complex functions are required in data processing and telecommunications devices, integrating them in small systems/packages increases. Complex arithmetic (subtraction, multiplication, division) relies on multiple adders. Adder performance affects the overall system. Two major methodologies improve adder performance:

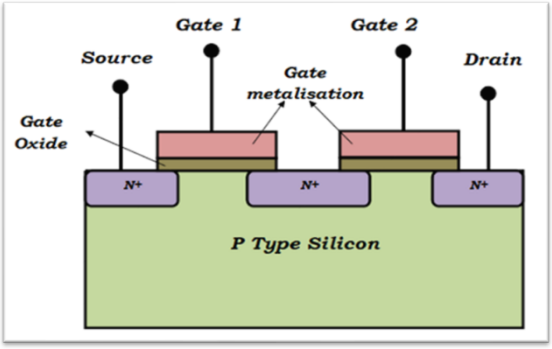
1. **Architecture viewpoint**: Shorten longest critical paths (often carry propagation to MSB) in multi-bit adders.
2. **Circuit design viewpoint**: Transistor-level high-performance full adder cores, focusing on minimum transistor count, low power, high throughput, full-swing output, driving capability, chip area, and layout regularity.

This work uses **Double Gate MOSFET (DG-MOSFET)** for both exact and approximate full adders, leveraging its advantages in nano-regime (reduced leakage, better SCE immunity) to enhance power/speed trade-offs.

II DOUBLE GATE MOSFET

Double Gate MOSFET is manufactured using Silicon on Insulator method. Silicon channel is grown over silicon oxide layer. It is like two FETs connected in series. The highly doped N middle block acts as the drain for the first FET and source for the second FET. The gate oxide between gate and the channel is the dielectric layer and the metal used for gate is conductor and the channel is also conductor, so all these three layers together form the capacitor. So, it is like two capacitors connected in series. The total capacitance

connected in series is lesser than the individual capacitance. Two gates are used to reduce the feedback capacitance at high frequencies. The voltages at both the gates controls the flow of current in the channel. There are four types of DGMOSFET stied gate symmetric DG, tied gate asymmetric DG, separated gate symmetric DG, and separated gate asymmetric DG. The asymmetrical DGMOSFET can be achieved by applying different gate voltages, by different oxide thickness for front and back gates, by different gate material work functions or by all the options. An MOSFET is a voltage-controlled FET which has a metal oxide gate electrode. The gate is attached to the metal of the MOS structure. The gate electrode is separated from the main type of semiconductor which can either be the n channel or p-channel by a thin insulating Dielectric layer of silicon dioxide.



Figue:1 Structure of Double Gate MOSFET

- Reduced subthreshold leakage (1–2 orders lower)
- Near-ideal subthreshold swing
- Higher I_ON due to volume inversion
- Robustness to process variations and delay fluctuations

FinFET (a DG variant) is widely adopted below 22 nm. DG-MOSFET suits low-power arithmetic in approximate designs.

III FULL ADDER BASICS

Full Adder is the adder that adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another. we use a full adder because when a carry-in bit is available, another 1-bit adder must be used since a 1-bit half-adder does not take a carry-in bit. A 1-bit full adder adds three operands and generates 2-bit results. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder. The logic diagram of Full adder is shown in the figure 2. The full adder uses 2 XOR gates for the calculation of its sum and 1 XOR, 1 OR and 2 AND gates for the calculation of carry out.

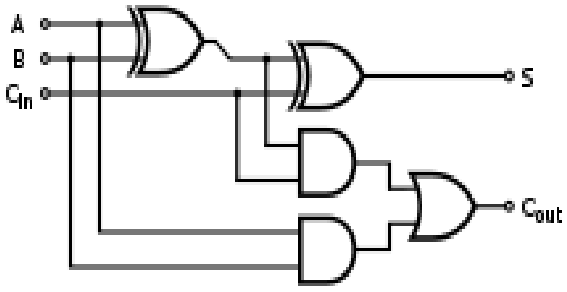


Figure 2: Logic Diagram of Full Adder

The full adder is usually a component in a cascade of adders, which add 8,16,32 etc. are binary numbers. The circuit produces a two-bit output sum represented by the signals Cout and Sum. The one-bit full adder's truth table is:

Table1: Truth Table of Full adder

Inputs			Outputs	
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A full adder can be implemented in many different ways such as with a custom transistor- level circuit or composed of other gates. In this implementation, the final OR gate before the carry-out output may be replaced by an XOR gate without altering the resulting logic. Using only two types of gates is convenient if the circuit is being implemented using simple IC chips which contain only one gate type per chip.
A full adder can be constructed from two half adders by connecting A and B to the input of one-half adder, connecting the sum from that to an input to the second adder, connecting Ci to the other input and OR the two carry outputs. Equivalently, S could be made the three-bit XOR of A, B and Ci and Cout could be made the three-bit majority function of A, B and Ci.

IV. PROPOSED FULL ADDER DESIGNS USING DG-MOSFET

DG- MOSFET full adder circuit has been designed using the equivalent style. DG-MOSFET will be constructed by connecting two single gate MOSFET transistors in parallel in such a way that their source and drain are connected together.

14 T Full Adder:

Double gate 14T full adder consists of 14 transistors to generate the sum and carry. It shows the 14T full adder. It consists of four transistor XOR structure, it is the fastest adder compared to 28T adder. The circuit is simpler than the conventional adder. The main disadvantage the power dissipation in this circuit is more than the 28T adder. However, with same power consumption it performs faster. The 14T adder with 14 transistors consumes considerably less power in the order of microwatts and has higher speed. The 14T adder reduces threshold loss problem compared to the previous different types of transistor adders. This adder cell uses 14 transistors to perform full adder operation as the name indicates. It uses hybrid logic style. It uses a XOR/XNOR circuit with feedback loop and transmission gates in its implementation. This adder has improved
output than single logic adders. This adder has reduced number of transistors and power dissipating nodes but it has less driving capability and noise immunity.

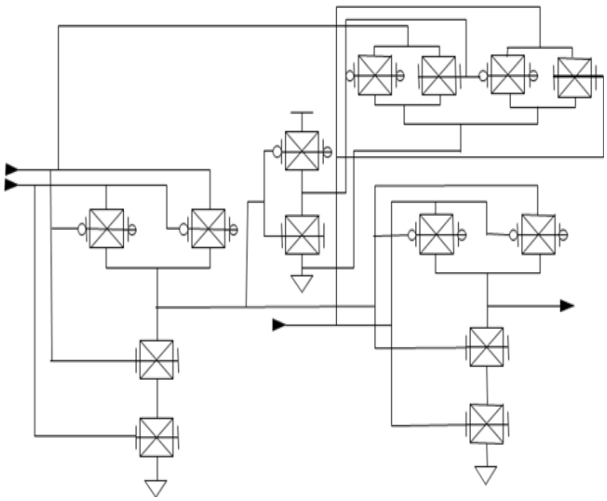


Figure 3:14T Full adder

Here we are designed 14T full adder by taking the two single gate MOSFETS are parallel together by connecting the sources and drain together.

10T Full Adder:

In this section one-bit full adder circuit is presented by using double gate transistors for improve the performance of adder in terms of power and leakage. This cell is made by using the 4T XOR gate. It is the essential component of full adder cell and generates the essential addition operation of adder cell. It behaves like a single half adder cell. Conventionally XOR gate use 8 MOSFETs for proper working, but present we have different topologies. Here we have used 4T XOR gate to increase circuit density. compare to 14T Using this XOR gate, reduction in size of full adder is achieved and overall leakage is also reduced.

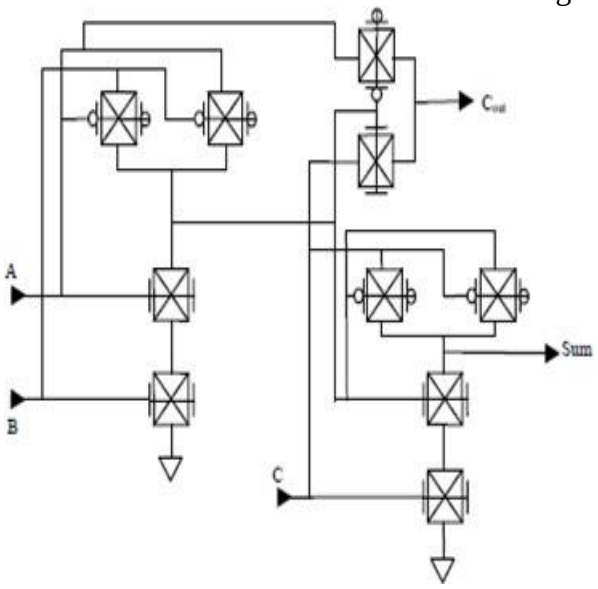


Figure 4:10T Full adder

6T Full Adder:

Numerous full adder circuit designs have been reported using reduced number of transistors as mentioned earlier. A full adder circuit with 6 transistors is presented which uses complementary inputs. Hence, requiring additional transistors to invert the input signals. Ultimately a novel 6T design is described in which requires non-complimentary inputs. Their design utilizes the new 2T XNOR gates. It is the essential component of full adder cell and generates the essential addition operation of adder cell. It behaves like a single half adder cell.

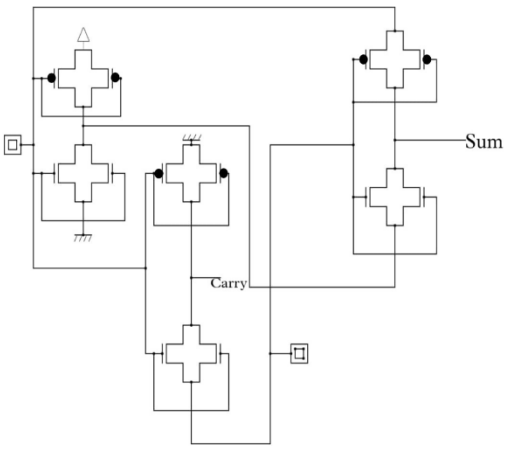


Figure 5 :6 T Full adder

It is the fastest adder compare to 10T and 14T adder. The circuit is simpler than the conventional adder.

V. SIMULATION SETUP AND RESULTS

Simulation is carryout by using Tanner Eda and Microwind .

Tanner EDA provides a complete line of software solutions for the design, layout and verification of analog and mixed-signal (A/MS) integrated circuits (ICs).Tanner's solution consists of tools for schematic

entry, circuit simulation, waveform probing, full-custom layout editing, placement and routing, netlist extraction, LVS and DRC verification.

Micro wind is a tool for designing and simulating circuits at layout level. The MICROWIND software allows the designer to simulate and design an integrated circuit at physical description level. Micro wind unifies schematic entry, pattern based simulator, SPICE extraction of schematic, Verilog extractor, layout compilation, on layout mix-signal circuit simulation, cross sectional & 3D viewer, netlist extraction, BSIM4 tutorial on MOS devices and sign- off correlation to deliver unmatched design performance and designer productivity. The package contains a library of common logic and analog ICs to view and simulate.

Design of 14T Full Adder:

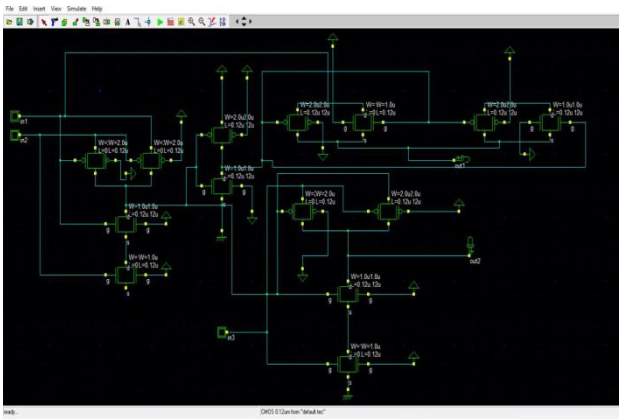


Figure 6: Schematic design of 14 T full adder using Double Gate MOSFET.

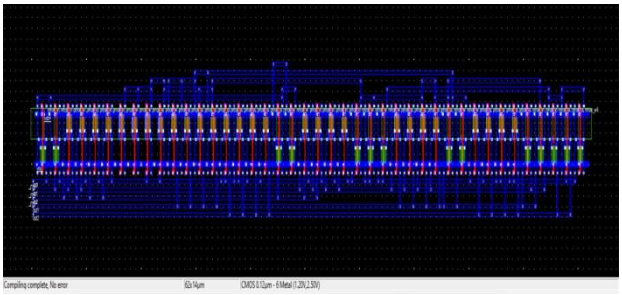


Figure 7:layout design of 14 T full adder using Double Gate MOSFET.

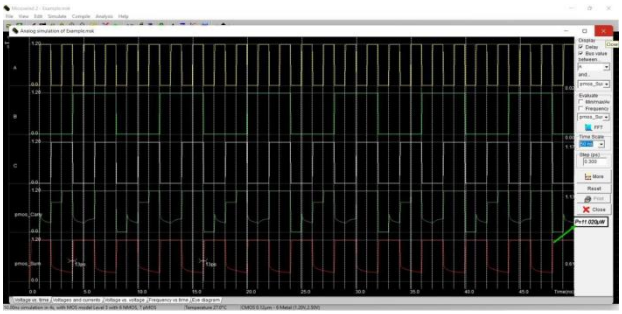


Figure 8: Simulation results of 14 T full adder using Double Gate MOSFET.

Design of 10 T Full Adder:

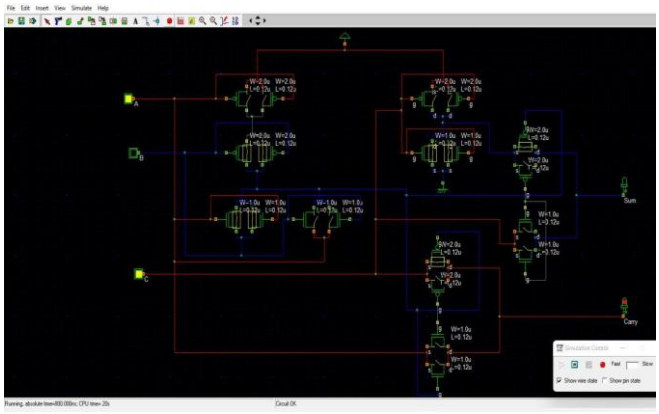


Fig.(a)

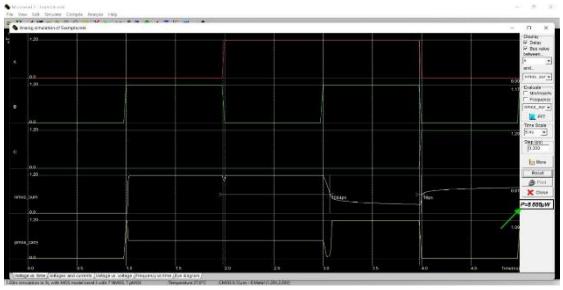


Fig.(b)

Figure 9: a)Schematic design and b) Layout Design of 10 T full adder using Double Gate MOSFET.

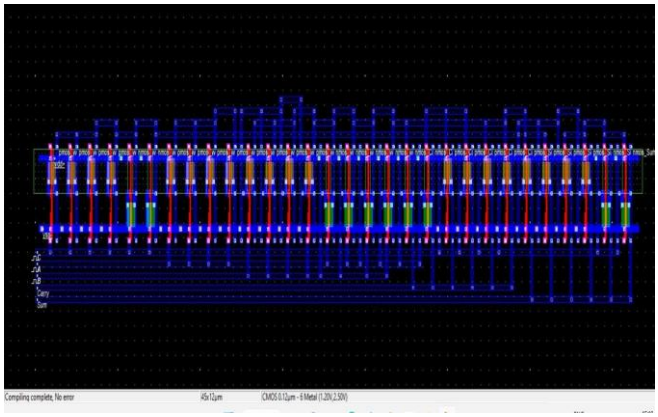


Figure 10: Simulation results of 10 T full adder using Double Gate MOSFET.

Design of 6 T Full Adder:

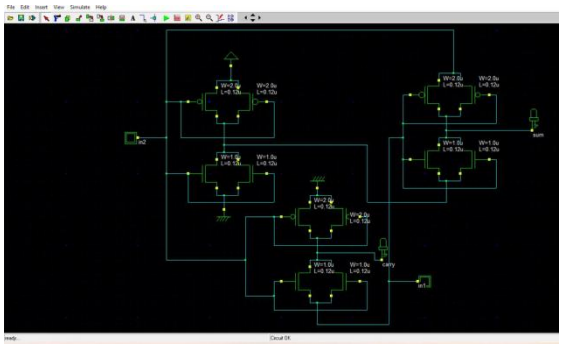


Fig.(a)

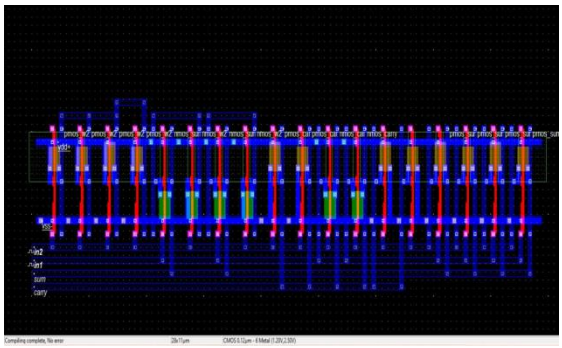


Fig.(b)

Figure 11: a)Schematic design and Layout Design of 6 T full adder using Double Gate MOSFET.

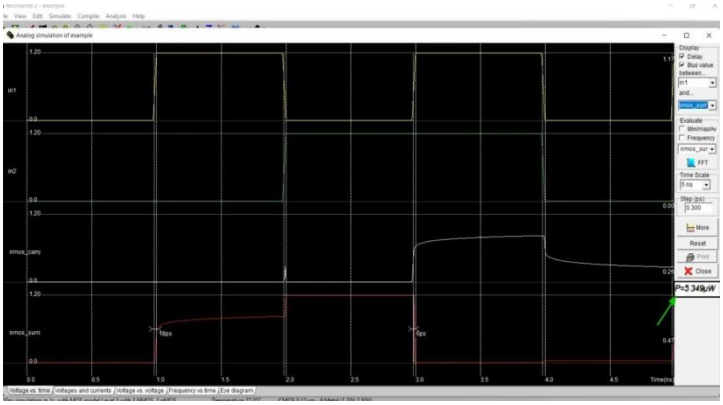


Figure 12: Simulation results of 6 T full adder using Double Gate MOSFET.

VI CONCLUSION

By analyzing we got the electrical characteristics and found that general MOSFET is affected by short channel effects like Barrier Lowering due to increase in drain voltage, impact ionization, ion scattering. If we place the source & drain closen together the FET will be more susceptible towards short channel effect. In double gate structure the parasitic capacitance is reduced quite remarkably. Through experimental result analysis, the Double Gate structure has many advantages over conventional Single Gate MOSFETs. A slight draw back in the Double Gate structure arises due to misalignments which can be optimized by careful design and simulation. There is also enhanced drain current output for DG FETs than conventional Single Gate MOSFETs. Overall, the electrical characteristics are better than conventional Single Gate MOSFETs. The simulation results shows that design is done with 6T, 10T and 14T dual gate 45nm transistor. The Proposed Circuit operation is Analyzed for all type of transistors and it is verified that circuit with 6 transistors is having less power consumption compared to other. Finally, we will conclude that, to increase the switching speed a reduced channel 6 transistor is used, by this power consumption is also reduced. Moreover DG-MOSFET reduces short channel effect which is a major concern.

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