

A 2.4 GHz Low Noise Amplifier in UMC 180 nm Technology

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Abstract— The Low Noise Amplifier (LNA) is typically the starting stage of an RF receiver. Its is used in the communication system to provide enough gain with minimum possible noise at receiver end. The objective of this work is to find out an innovative design idea for LNA to obtain improved performance over the traditional design. The LNA Circuit designed here is for Wireless Local Area Network (WLAN) application i.e. 2.4 GHz. The main LNA constraints are Gain, Noise Figure (NF) and power consumption. In this paper the LNA is presented with Inductive degenerated topology using cascoded dual CMOS architecture for obtaining the improved LNA constraints. The LNA design is simulated in Cadence Virtuoso IC tool using 180nm technology. The results of the simulation shows that the gain is 12.35 dB, input return loss (S_{11}) of -6.842 dB, reverse isolation (S_{12}) of -32.9 dB, S_{22} equals to -0.611 dB. It produces a Noise Figure (NF) of 0.281 dB and corresponding Noise Factor is 1.0068. This proposed LNA circuit operates at supply voltage of 1.8v.**Keywords**

Index Terms— Noise Figure, Cascoded LNA, Inductive degeneration, Radio frequency(RF)

I. INTRODUCTION

The Wireless Communication has always been attracting the interest of researchers because of the growth in its uses such as mobiles(phones), WLAN and remote receivers. This increase in demand of these devices motivates us to work on designing the optimized circuits.

The Low Noise Amplifier(LNA) is the starting stage of the receiver front-end after the antenna and it is used to increase the signal power that is incoming from antenna. In addition to this amplification the some noise has also been added to the incoming signal. So, the target of this work is to achieve a design idea which allows a significant gain with lowest possible noise addition. In addition to that it should also show a specific impedance, such as 50 Ohm to the input source[1]. For this purpose this paper presents a cascoded CMOS LNA using the inductor degeneration topology.

II. DESIGN METHODOLOGY

The designing of Low Noise Amplifier is the trade off among its gain, noise, power, input and output matching and linearity.

In Spite of having very low power consumption and less area occupied in single-ended input architecture, the use of differential-ended input architecture is preferred whose power consumption is approximately double because its ability towards noise and linearity performance. Moreover, the single ended Low Noise Amplifier architecture is sensitive towards parasitic ground inductance and there is difference in the same potential at different points. The differential input LNA has the quality to cancel out the even-order harmonics which improves the linearity. The dynamic range of the circuit also increases in differential architecture [2]. These are the main reason for going with the differential input architecture for the LNA design.

A. Cascoded LNA Design

The cascade structure is popular used in LNA for narrow-band wireless applications. It is two-stage amplifier consisting of common gate (CS-CG) stages.

The most common used topology in the design of LNA is the common source topology. A source inductor included can move the value of input voltage reflection coefficient of LNA closer to the optimized value of transmission coefficient which can thereby help in obtaining a minimum value of noise figure and good input return loss simultaneously [3].

B. Traditional Differential LNA circuit design

The traditional design for differential LNA circuit with inductive degeneration and common source topology is shown in figure1.

The optimum value of all the components used in the circuit help in achieving the better performance. M1 and M3 are the main transistors while M0 and M2 are cascading transistors. L8 and L9 are degenerated inductors, L3 and L4 are source inductors and L2 and L5 are drain inductors.

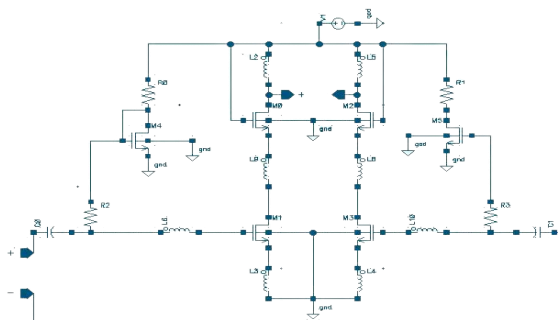


Table 1

Design Constraints	Desired values
Frequency	2.4 GHz
Technology	180 nm
Vdd	1.8 V
Noise Figure	<3.14
Gain	>12dB

Figure 1 Traditional LNA

C. LNA Design Constraints

Table 1 shown below depicts the design constraints used by this LNA design. The LNA designed for WLAN application must meet the required desired specifications like frequency of operation should be 2.4 GHz for because mostly WLAN operations prefer this operating frequency, the technology we allowed by our designing software available is 180 nm, the Noise figure achieved till now is 3.14 so our aim is to minimize this figure with the gain to be maintained in the acceptable Range that is greater then 12 dB. The acceptable operating voltage is 1.8 V.

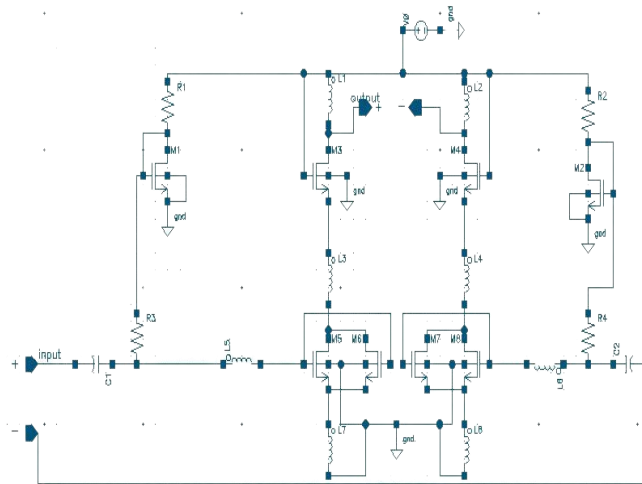


Figure 2 Proposed LNA Design

III. PROPOSED LNA DESIGN

As the differential topology approach is usually preferred in the radio frequency (RF) design due to its well known characteristics of immunity to common mode disturbances, rejection to parasitic couplings, and increased dynamic range.

The proposed design for the cascaded dual CMOS LNA is shown below in Fig. 2. Here each common source (CS) stage of cascade structure is made by connecting two transistors in parallel instead of one.

The transistors M5-M6 and M7-M8 are the common source transistors. M3 and M4 are common gate(CG) transistors, L3 and L4 are inter-stage inductors. L1 and L2 are the drain inductors at output end and L5-L6 are the gate inductor at input end. L7 and L8 are the source inductors. These inductors at input and output ends play a major role in the impedance matching.

The cascading transistor M3 and M4 reduce the interaction of the tuned output with the tuned input. The proposed design has increased complexity in a differential structure, But the degree of design choice is satisfied with the objectives such as gain and most importantly the noise Figure.

For obtaining the desired performance there is a requirement of a biasing circuit in order to that M1 and M2 are the biasing transistors with four resistors R1-R2 and R3-R4 are providing the biasing current to the circuit.

Table 2

Device	Parameter
M1, M2	10µm/0.18µm
M3, M4	300µm/0.18µm
M5, M6, M7, M8	150µm/0.18µm
L1, L2	4nH
L3, L4	7.5nH
L5, L6	7nH
L7, L8	3nH
R1, R2	1K
R3, R4	2K
C1, C2	15pF

A. Components Parameters

The Table shown here parameters.

In table the M1- M8 represents the transistors used, R1- R4 are two resistors used in the

IV. SIMULATION RESULTS FOR

The Simulation of the Cadence Spectre IC tool. The design is observed by s-figures below:

of the Proposed LNA Design summarizes the component

the eight transistors, L1- L8 R4 are the resistors and C1 & C2 proposed design.

THE PROPOSED LNA proposed design is done in the performance of the proposed parameters. As shown in the

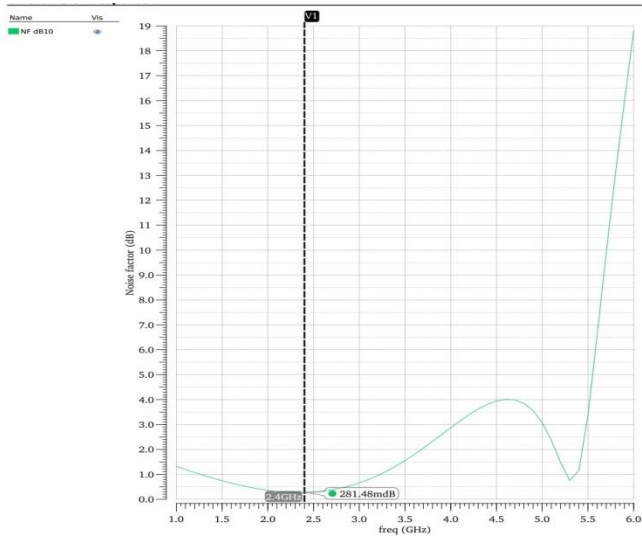


Figure 3 Simulated result for Noise Figure

Gain (S_{21})

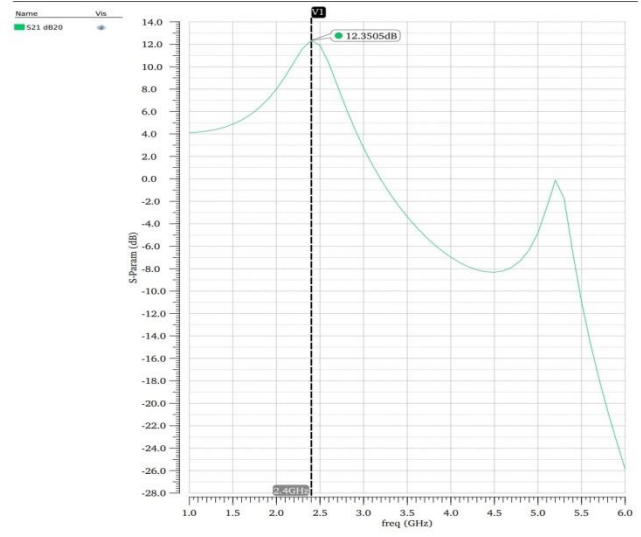


Figure 4 Simulated result for Power

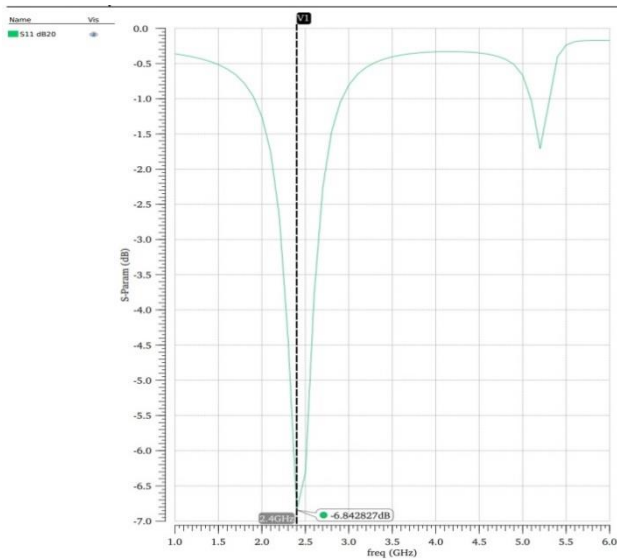


Figure 5 Simulated results for S_{11} (input return loss)

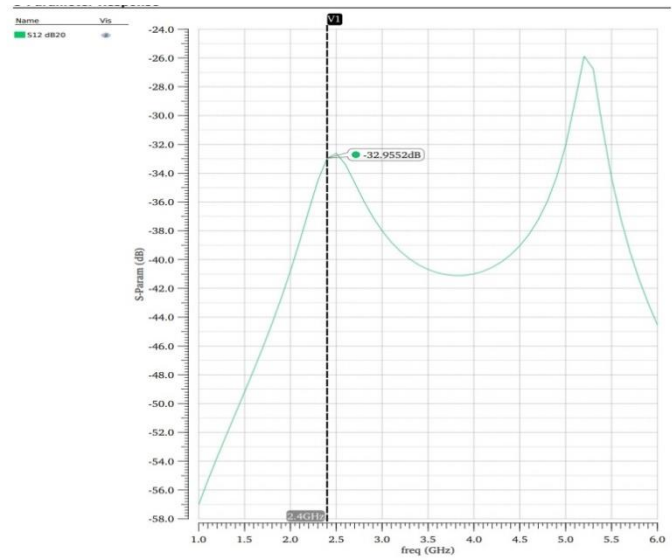


Figure 6 Simulated results for S_{12} (Reverse Isolation)

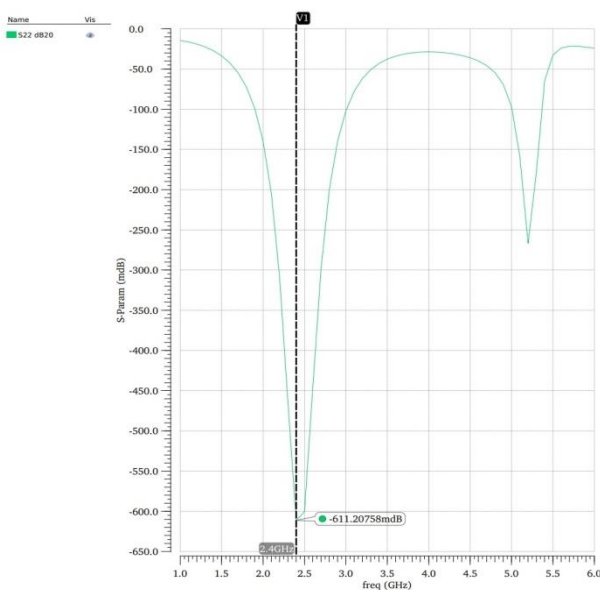


Figure 7 Simulation results for S_{22} (output reflection loss)

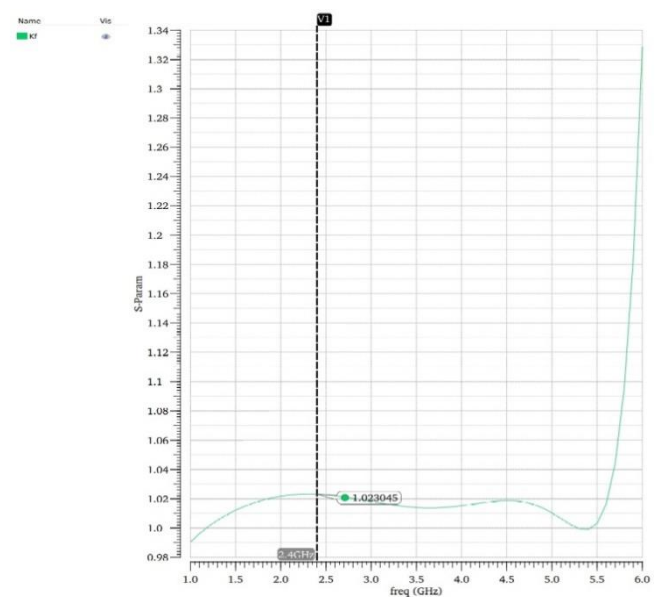


Figure 8 Simulated result for K_f

Table 3

<i>Parameter</i>	<i>This work</i>	<i>[2]</i>
Frequency (GHz)	2.4	2.4
S ₁₁ (input return loss) (dB)	-6.842	-13.5
S ₁₂ (reverse isolation) (dB)	-32.9	-33.85
S ₂₁ (power gain) (dB)	12.35	12.68
S ₂₂ (output reflection loss) (dB)	-0.611	-10
Noise Figure (dB)	0.281	3.14
NF _{min} (dB)	0.267	1.9
CMOS Process	180nm	180nm
K _f	1.023	4.84
Supply Voltage (V)	1.8	1.8

The Designing of proposed Low Noise Amplifier circuit is done using 180nm technology on the Cadence Virtuoso IC Design tool. The Simulation for the proposed circuit was performed using Cadence Spectre IC tool. The obtained results are shown in the above figures. The achieved noise figure value is 0.281dB and the power gain is 12.35 dB.

The table shown here gives a comparative analysis of the performance parameters the traditional LNA and the proposed LNA design.

V. CONCLUSION

The proposed Design provides a balance in performance among the Noise Figure and Power gain. The Noise Figure in the proposed design is reduced to 0.281 from the 3.14 in [2], with provided gain as 12.35 dB and stability factor K_f in the acceptable range i.e. greater than 1. The reverse isolation S₁₂ is also high so that the leakage is low. The Design and Simulation of the proposed circuit is done by Using UMC 180 nm CMOS RF Process on Cadence Virtuoso IC Design tool. The power gain obtained from the proposed design is 12.35 dB with a Noise Figure value of 0.281dB and NF_{min} as 0.267dB. The noise factor for this circuit is 1.06684. The power supply used for simulation of the proposed circuit is 1.8 V. This design idea can also be used for designing the LNAs for some other frequencies say 5GHz by making trade off between the inductor and capacitor values.

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