Design of Front End Optical Receiver using CMOS 180nm Technology

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Abstract: This paper presents design of front end optical receiver using CMOS 180nm technology. After completion of its schematic view, simulation is done through Cadence Virtuoso tool. In this design the power supply used by authors is 1.8V and frequency range between 1Hz to 10GHz is used and obtained results in various parameters like 20µA bias current, aspect ratio W/L, input common mode voltage range lying between 800mv and 1.72volts.The trade-off among various parameters such as open loop gain are measured and the trade-off among parameters such as open loop gain, Phase margin are measured. The overall gain is obtained as 98 dB. The simulation results are reported in this paper.

Index Terms: Analog circuit, Two stage operational amplifier, Aspect Ratio, 180nm, Optical Receiver, CADENCE.

I. INTRODUCTION

Day by day the requirement for large Bandwidth for interconnecting cable technology is increasing [1]. There is an increased interest in high speed Optoelectronics devices and systems in present day scenarios as the volume of telecommunications data has grown rapidly. The data traffic have increased very fastly as most of today's traffic is over the internet. The first building block in the receiver design for optical communication after Photodiode is transimpedance amplifier(TIA) which converts the incoming photo diode current(PD) in to voltage signal that is to be used in the digital processing units[2].

The TIA characteristics should have a low input referred current noise to enlarge or maximize the overall receiver sensitivity and reduce the noise from succeeding stages [3]. Moreover, there is a huge requirement of large Bandwidth of the TIA which is enough for the required bit rate in order to minimize the inter-symbol interference (lSI). In this paper, authors present a front end optical receiver designed with almost GHz bandwidth range and 98 dB transimpedance gain suitable for 10 Gbps optical receiver applications using 180 nm CMOS technology.

II. CIRCUIT ARCHITECTURE

The figure depicted below shows the circuit architecture of a basic optical receiver circuit. The current coming from the external photodiode (PD) is converted to an output voltage signal and amplification of data is done. A Post Amplifier is also used in cascade to TIA, which provides more gain for the circuit with sufficient gain. The output driver is designed with the consideration for chip-to-chip interconnection. Here the Post Amplifier used is an Operational Amplifier to provide large gain to circuit.

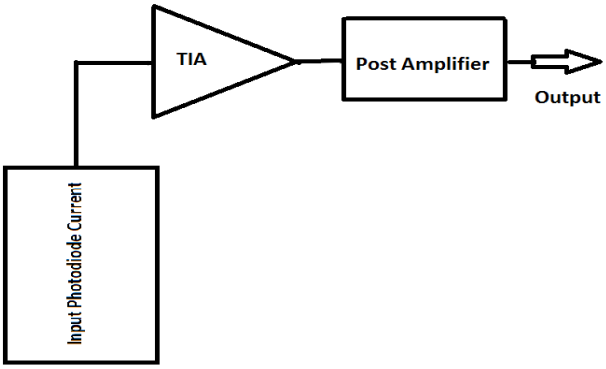


Fig.1- Block Diagram of basic optical receiver circuit.

TIA Structure

Fig. 2 shows Regulated-Cascode transimpedance amplifier(RGC TIA) and Fig. 3 depicts Shunt-Feedback transimpedance amplifier (SF TIA), respectively.

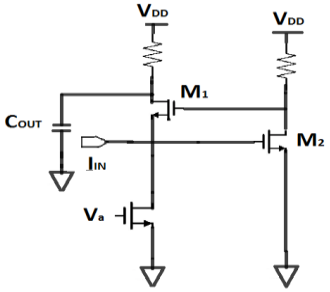


Fig.2- Regulated Cascode Transimpedance Amplifier.

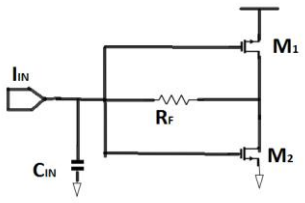


Fig.3- Shunt-feedback Transimpedance amplifier

The gain bandwidth product (GBW) of the two TIAs is analyzed in equations (1) and (2). It is found that the gain bandwidth of Shunt Feedback TIA is proportionate to trans-conductance parameter gm, which is lesser than other short length process. Thus, in this paper, RGC TIA methodology is adopted in TIA designing except clock channel which will thereby require less area in occupation.

$$GBW(RGC) = \frac{1}{2\pi RfCd1} * Rf = \frac{1}{2\pi Cd1} \quad (1)$$

$$GBW(SF) = \frac{gmro * Rf}{2\pi Cin(Rf + r0)} = \frac{gm(Rf||r0)}{2\pi Cin} \quad (2)$$

III. PROPOSED DESIGN IMPLEMENTATION

TIA Methodology

The proposed designed architecture of first block of optical receiver circuit i.e. Transimpedance amplifier is shown using 180nm technology. Four NMOS and two PMOS used in the design strategy of TIA. Region of operation of these MOSFET's are chosen to obtain the desired gain and phase specifications and to maximize the gain of overall circuitry.

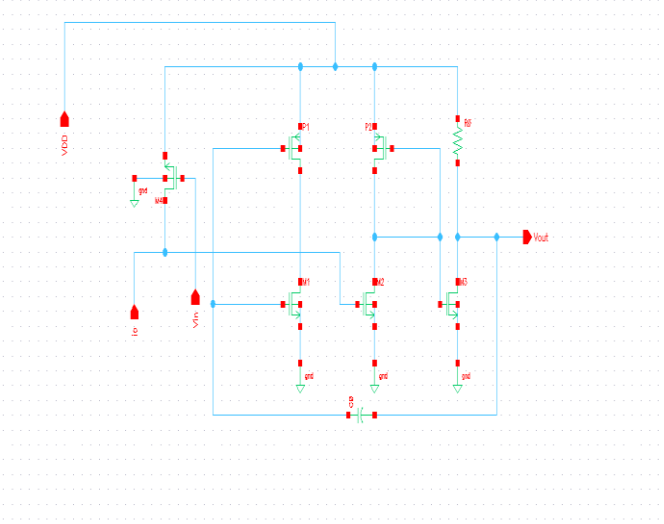


Fig.4- Schematic design of Transimpedance Amplifier

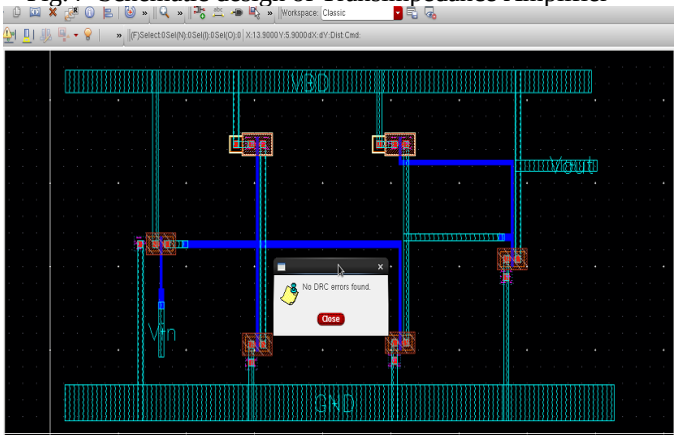


Fig.5- Layout of proposed TIA structure with no DRC errors in Cadence Virtuoso Tool.

Figure 5 above represents the layout of Transimpedance amplifier. Metal to Metal connections were made to short the Drain and Source of the MOSFET. Via is created to connect the Gate and Source or Gate and Drain. No DRC errors were found while performing the Design Rule Check in Cadence tool.

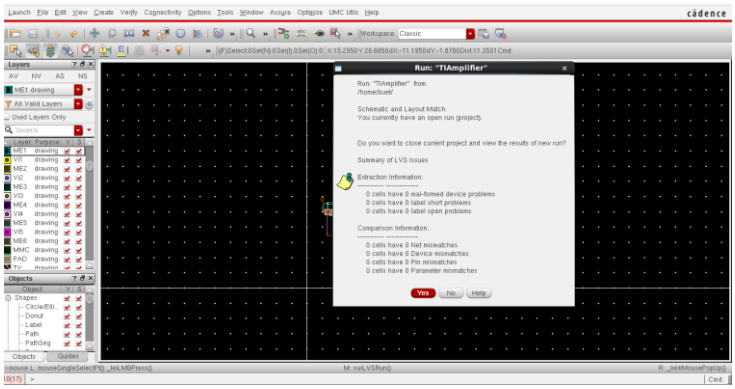


Fig.6 -Layout versus Schematic result of proposed TIA architecture.

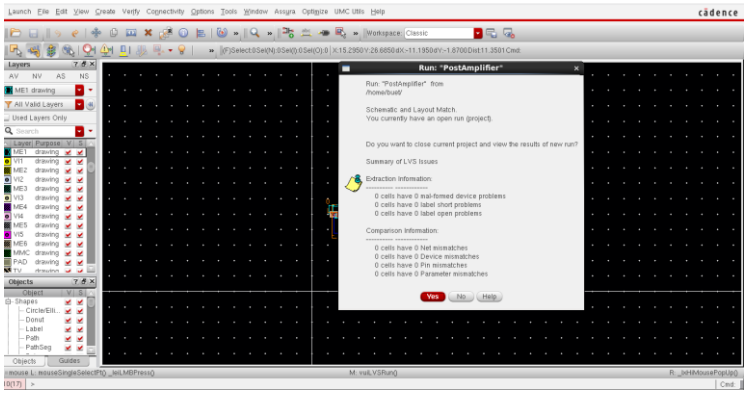


Fig.7 - Layout versus Schematic result of proposed Post Amplifier architecture.

Figure 6 and Figure 7 respectively shows layout versus schematic (LVS) of proposed transimpedance amplifier and post amplifier i.e. Operational amplifier used here. LVS match as all the devices and nets of the schematic are matching with the nets of layout structure.

Post Amplifier (Operational Amplifier) Methodology

This section includes the design strategy for Post Amplifier which is Op-Amp. The supply voltage specification used is 1.8V power supply. This post amplifier provides higher gain and thus the overall cascaded gain is improved and hence can be used for desired applications.

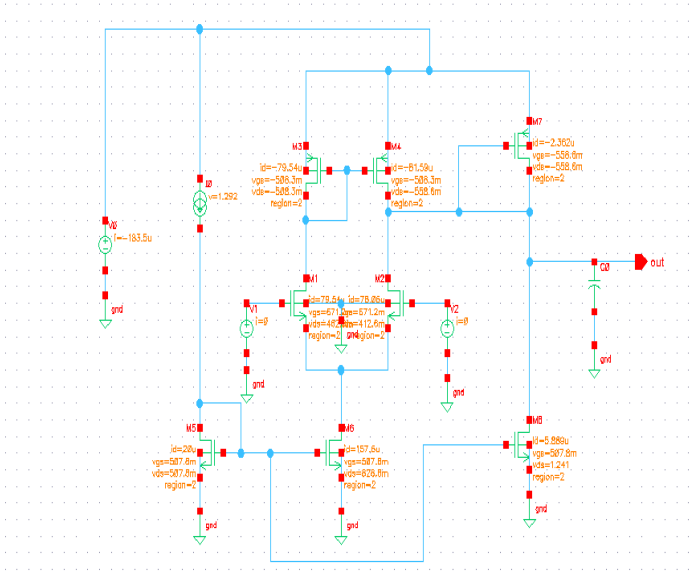


Fig.6- Schematic of proposed Post Amplifier (Operational Amplifier)

This design includes 5 NMOS and 3 PMOS in the circuitry. All the MOSFET's are designed to operate in Region 2 i.e. Saturation region. The input voltage values were taken in between 800mV and 1.6V. The best desired results are obtained for input voltage being 1.5V. The W/L ratios taken for MOSFET's are different to get the desired results.

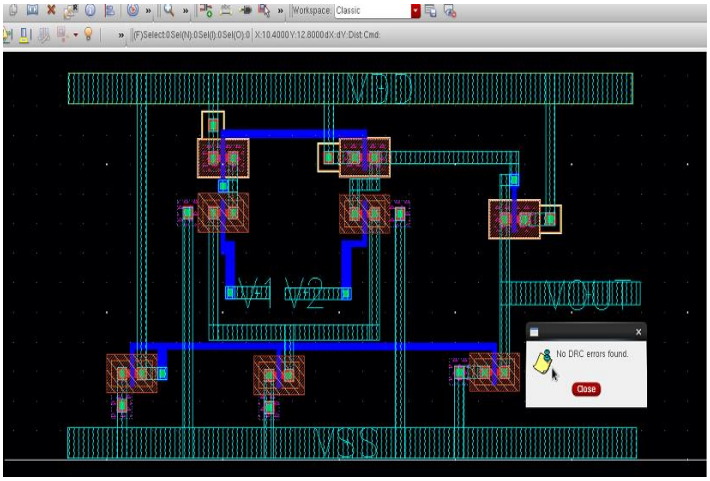
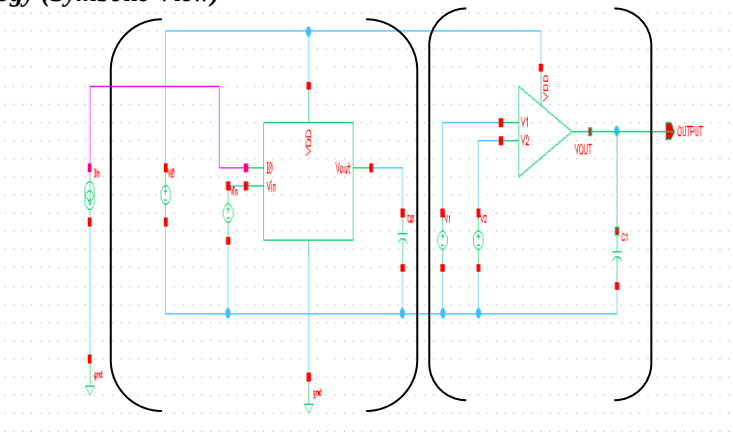


Fig. 7- Layout of proposed post amplifier (Op-Amp) structure with no DRC errors in Cadence Virtuoso Tool.

Figure 7 represents the layout of Post Amplifier(Op-Amp). No DRC errors were found while performing the Design Rule Check in Cadence tool.

Cascaded Structure Methodology (Symbolic View)



TIA SYMBOL POST AMP. SYMBOL

Fig.8 - Cascade Structure of Proposed TIA and Post Amplifier design using Cadence Virtuoso tool.

IV. SIMULATION RESULTS

The supply voltage is taken to be 1.8V and the incoming Photodiode current is taken of magnitude 20uA. Different values of aspect ratio are taken for each MOSFET's and the results are obtained. The frequency responses of TIA and post amplifier(operational amplifier) is shown below.

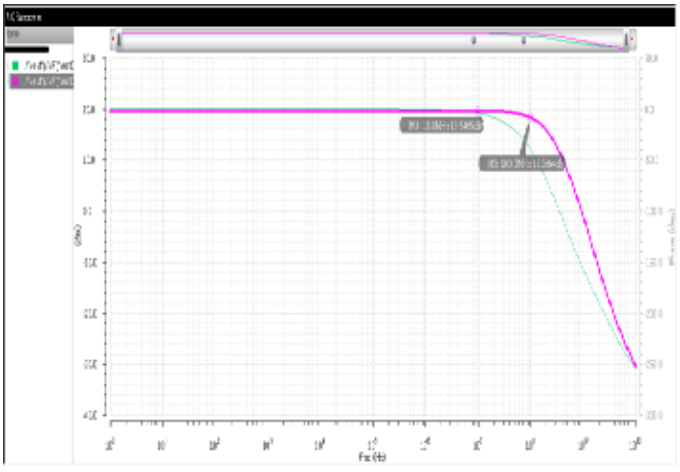


Fig.9- Gain and Phase response of proposed TIA architecture.

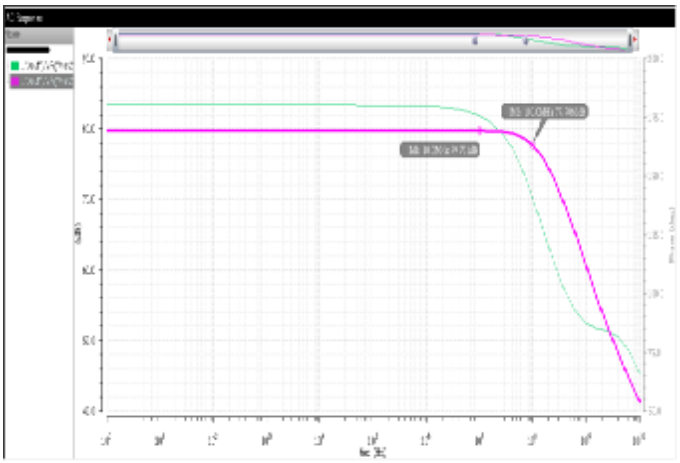


Fig.10- Gain and Phase response of proposed Post Amplifier.

Fig. 9 and Fig. 10 depict the gain and phase frequency response obtained for proposed TIA and proposed post amplifier respectively. This design has been carried out in Cadence Virtuoso tool lab.

V. CONCLUSIONS

This paper explains the design of a front end optical receiver using 180nm CMOS Technology in Cadence Virtuoso Tool. The gain obtained was around 98 dB and bandwidth obtained was almost GHz range.

Below shown is the comparison table for various parameters.

Table 1 Table showing comparison of conventional and proposed work.

Reference	[1]	This Work
Process Technology	180nm	180nm
Main Topology	RGC-TIA	RGC-TIA
Input Current (µA)	-	20
Supply Voltage (V)	1.8	1.8
Transimpedance Gain (dBΩ)	78	98
Cpd (pf)	-	0.1
Power(mW/channel)	54	47

Thus suitable efforts are made to obtain the desired values of Gain, Phase and Power consumption. Suitable techniques are used comparatively both in designing of Transimpedance amplifier and Post amplifier which here used is an Operational amplifier, using Cadence Virtuoso Tool.

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