Physical Design of Low Power Operational Amplifier

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***Abstract*: A CMOS single output two stage operational amplifier is presented which operates at 3 V power supply at 0.18 micron (i.e., 180 nm) technology. It is designed to meet a set of provided specifications. The unique behavior of the MOS transistors in sub- threshold region not only allows a designer to work at low input bias current but also at low voltage. This op-amp has very low standby power consumption with a high driving capability and operates at low voltage so that the circuit operates at low power. The op-amp provides a gain of 20.4dB and a -3db bandwidth of 202 kHz and a unity gain bandwidth of 2.15MHz for a load of 5 pF capacitor. This op-amp has a PSRR (+) of 85.0 dB and a PSRR (-) of 60.0 dB. It has a CMRR (dc) of -64.4 dB, and an output slew rate of 12.465 v/µs. The power consumption for the op-amp is 1.18mW. The presented op-amp has a Input Common Mode Range(ICMR) of -1V to 2.4V. The op-amp is designed in the 180 nm technology using the umc 180 nm technology library. The layout for the above op- amp had been designed and the post layout simulations are compared with the schematic simulations.**

***Keywords*: Scientific writing, Technical writing, Journal article, FET, MOSFET**

I.INTRODUCTION

The operational amplifier is undoubtedly one of the most useful devices in analog electronic circuitry. Op-amps are built with vastly different levels of complexity to be used to realize functions ranging from a simple dc bias generation to high speed amplifications or filtering.With only a handful of external components, it can perform a wide variety of analog signal processing tasks. Op-amps are among the most widely used electronic devices today, being used ina vast array of consumer, industrial, and scientific devices. Operational Amplifiers, more commonly known as Op-amps, are among the most widely used building blocks in Analog Electronic Circuits. Op-amps are used equally in both analog and digital circuits. [1,2]

Op-amps are linear devices which has nearly all the properties required for not only ideal DC amplification but is used extensively for signal conditioning, filtering and for performingmathematical operations such as addition, subtraction, integration, differentiation etc . Generally an Operational Amplifier is a 3-terminal device. It consists mainly of an Inverting input denoted by a negative sign, ("-") and the other a Non-inverting input denoted by a positive sign ("+") inthe symbol for op-amp. Both these inputs are very high impedance. The output signal of an Operational Amplifier is the magnified difference between the two input signals or in other wordsthe amplified differential input. Generally the input stage of an Operational Amplifier is often a differential amplifier.[3]

1.1 System Overview

For Op-amps used in many useful applications, rather a surprisingly large number of applications, the actual amplifier performance is closely approximated by an idealized amplifier model. Indeed quite frequently circuits are designed explicitly to insure acceptabilityof this approximation. And in other cases where the idealization is not a sufficiently accurate approximation nevertheless it often provides a starting point for an iterative process towards a final design. Consider the 741 amplifier, an older but proven industry-standard device, which has a voltage gain exceeding 105 in normal operation. To cause an output voltage change between representative saturation voltage limits of ±15 volts, A basic op-amp consists of 4 main blocks

a. Current Mirror
b. Differential Amplifier
c. Level shift, differential to single ended gain stage
d. Output buffer

The general structure of op-amp is as shown in figure 1 below:-

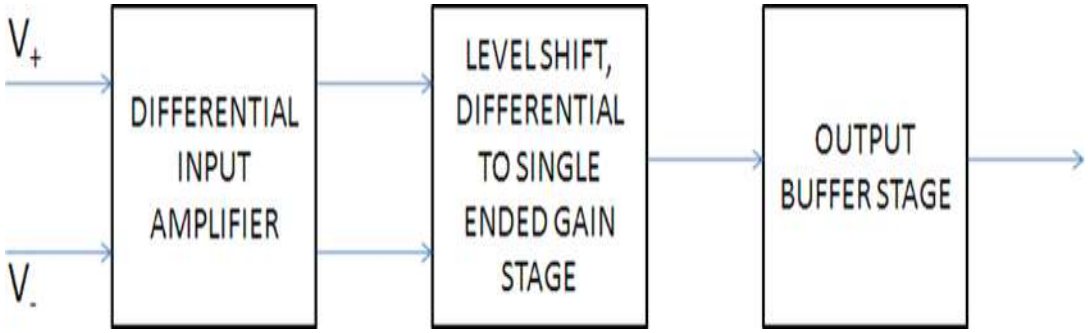

Figure 1: General Structure of op-amp

The first block is input differential amplifier, which is designed so that it provides very highinput impedance, a large CMRR and PSRR, a low offset voltage, low noise and high gain. The second stage performs Level shifting, added gain and differential to single ended converter. The third block is the output buffer. The output buffer may sometimes be omitted to form a high output resistance un-buffered op-amp often referred to as Operational transconductance amplifier or an OTA. Those which have the final output buffer stage have a low output resistance (Voltage operational amplifiers).[11-12]

II. LITERATURE SURVEY

Existing PLC Implementations:
The existing power line communication being implemented at various places and enumeration of standards evolved. In Europe PLC is termed as narrow band PLC because allocated frequency band for PLC is 3 KHz to 148.5 KHz, which is further divided into four sub-bands for different applications.

- CENELEC A (9 KHz to 95 KHz)
- CENELEC B (95 KHz to 125 KHz)
- CENELEC C (125 KHz to 140 KHz)
- CENELEC D (140 KHz to 148.5 KHz)

Details of operation in different bands such as type of modulation, data rate, symbol size and encoding-decoding technique are enlisted in [8]. CENELEC the controlling body of PLC mechanism in Europe, follows the Standards EN 50065 (CENELEC), IEC 61000. In China PLC operates at a single frequency band of 3 to 500 KHz. The frequency band in USA for PLC purpose is FCC band 10 KHz – 490 KHz. There is only single band with no subdivisions.

Op Amps For Everyone; 5th Ed; Bruce Carter, Ron Mancini; Newness; 484 pages; 2017; ISBN 978-0128116487. (2 MB PDF - 1st edition)

Operational Amplifiers - Theory and Design; 3rd Ed; Johan Huijsing; Springer; 423 pages; 2017; ISBN 978-3319281261.

Operational Amplifiers and Linear Integrated Circuits - Theory and Application; 3rd Ed; James Fiore; Creative Commons; 589 pages; 2016.(13 MB PDF Text)(2 MB PDF Lab)

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III.METHODOLOGY

An operational amplifier is often called an op-amp. It is a DC-coupled differential input voltage amplifier with an rather high gain. In most general purpose op-amps there is a single ended output. Usually an op-amp produces an output voltage a million times larger than the voltage difference across its two input terminals. Thus for an ideal op-amp the input signal is almost always a differential signal and hence a differential amplifier is generally used as the input stage of an Operational Amplifier. However, the infinite gain or bandwidth that characterizes an ideal operational amplifier is seldom found in a real Operational Amplifiers like the widely used uA741. Typically the "Open Loop Gain" of a real operational amplifier is defined as the amplifiers.

A.PRINCIPAL OF OPERATION

An op-amp has a differential input and single ended output. So, if we apply two signals one at the inverting and another at the non-inverting terminal, an ideal op-amp will amplify the difference between the two applied input signals. We call this difference between two input signals as the differential input voltage. The equation below gives the output of an operational amplifier.

Vout= Aol(V1-V2)

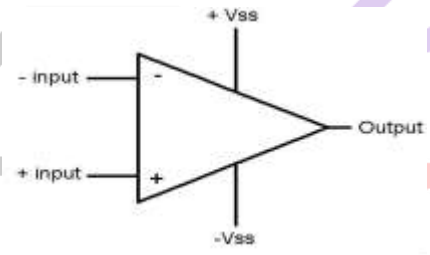
Where, V_{OUT} is the voltage at the output terminal of the op-amp. A_{OL} is the open-loop gain for the given op-amp and is constant (ideally). For the IC 741 A_{OL} is 2 x 10^5.
V1 is the voltage at the non-inverting terminal.V2 is the voltage at the inverting terminal.
(V1-V2) is the differential input voltage.
It is clear from the above equation that the output will be non-zero if and only if the differential input voltage is non-zero (V_1 and V_2 are not equal), and will be zero if both V_1 and V_2 are equal. Note that this is an ideal condition, practically there are small imbalances in the op-amp. Also, it is true that if we apply small differential input voltage, the operational amplifier amplifies it to a considerable value but this significant value at the output cannot go beyond the supply voltage of the op-amp. Hence it does not violate the law of conservation of energy.

B. ANALYSIS OF NON LINEAR IMPERFECTION

Output voltage is limited to a minimum and maximum value close to the power supply voltage. The amplifier's output voltage reaches its maxim slewing occurs, further increases in the input signal have no effect on the rate of change of the output. Slewing is usually caused by the input stage saturating rate of change, the slew rate, usually specified in volts per microsecond (V/μs). The output voltage may not be accurately proportional to the difference between the input voltages. It is commonly called distortion when the input signal is a waveform. This effect will be very small in a practical circuit where substantial negative feedback is used. The output current must be finite. In practice, most op amps are designed to limit the output current so as not to exceed a specified level – around 25 mA for a type 741 IC op amp – thus protecting the op amp and associated circuitry from damage. Modern integrated FET or MOSFET op amps approximate more closely the ideal op amp than bipolar ICs when it comes to input impedance and input bias currents. Bipolar are generally better when it comes to input *voltage* offset, and often have lower noise. Generally, at room temperature, with a fairly large signal, and limited bandwidth, FET and MOSFET op amps now offer better performance.

IV.OPERATIONAL AMPLIFIER

The general operational amplifier symbol is as shown in Figure 2 below:-
Equivalent Circuit Of An Op-AMP



An equivalent op-amp circuit is shown in the circuit below. It consists of two inputs often referred to as the inverting and non-inverting inputs. The input resistance or rather impedanceis referred in the diagram as Z_{in} and the output impedance is given by Z_{out}. This is the basic block diagram of a op-amp which generally has a single output.

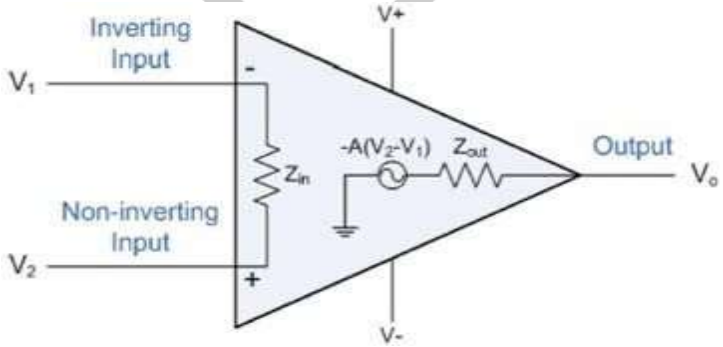


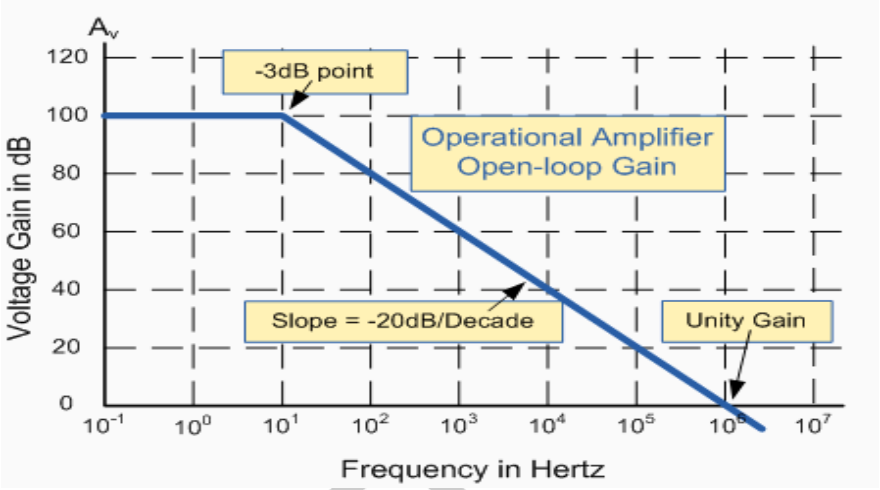
Figure 3: Equivalent Circuit for ideal operational amplifier

Idealized Characteristics

(a) Voltage Gain, (A) **Infinite**
(b) Input impedance (Z_{in}) **Infinite**
(c) Output impedance, (Z_{out}) **Zero**
(d) Bandwidth, (BW) **Infinite**
(e) Offset Voltage, (V_o) **Zero**

Open Loop Frequency Response Curve

VII.RESULT & DISCUSSION



The designed op-amp was simulated to find the different characteristics of the designed op-amp. Further the layout of the designed op-amp was created and the parasitic capacitance and resistance was extracted. The extracted designs were then simulated with the parasitic values and compared with the schematic. Later in the chapter we also compare the obtained parameters of the device through simulation to the specifications for the device and with the post layout simulation results. The different results are presented here.

Offset Voltage

It is the voltage obtained at the output terminals, when the input terminals are connected to ground terminal, i.e., 0 volts. Here the offset voltage calculated for the op-amp is -603mv.

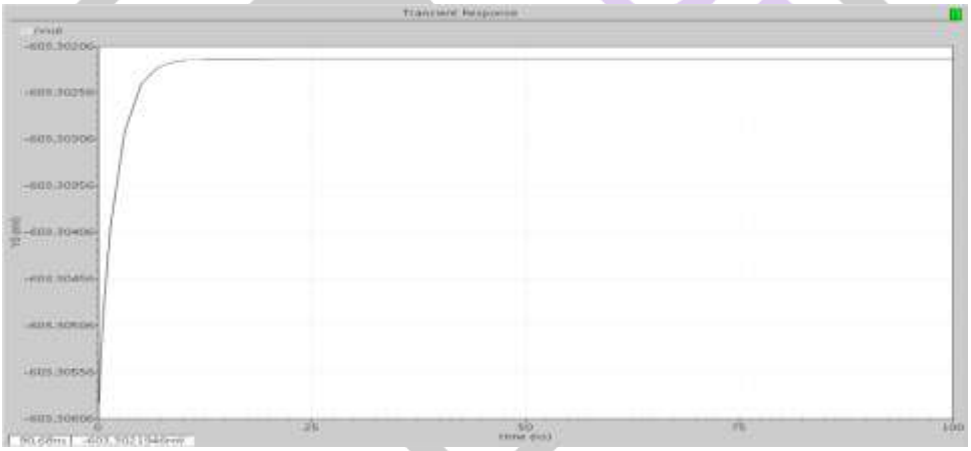


Figure 4: Op-Amp offset voltage

Slew Rate

It is the maximum rate of change of output voltage. Here the slope of the curve calculated as 12.5 v/µs.

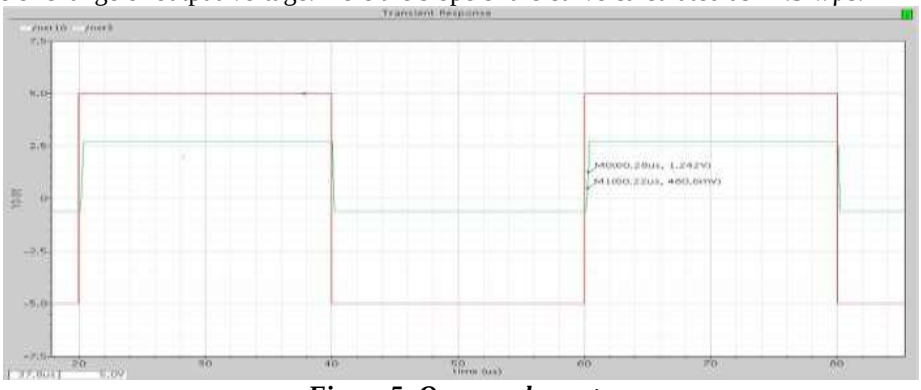


Figure 5: Op-amp slew rate

Gain

It is defined as the ratio of the output to the input. Here the input voltage given as 1 volts sinewave. Hence the gain is calculated as 10.4v/v.

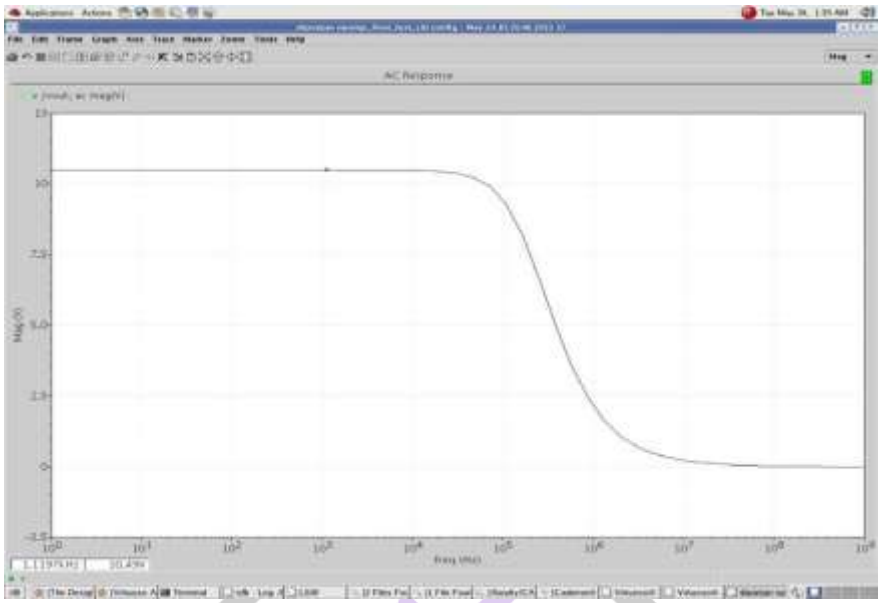


Figure 6: Op-Amp Gain

Bandwidth

It is the maximum allowable range of the frequencies. Here the bandwidth of this op-ampcalculated as 2.16 MHz for unity gain and 202kHz at -3dB.

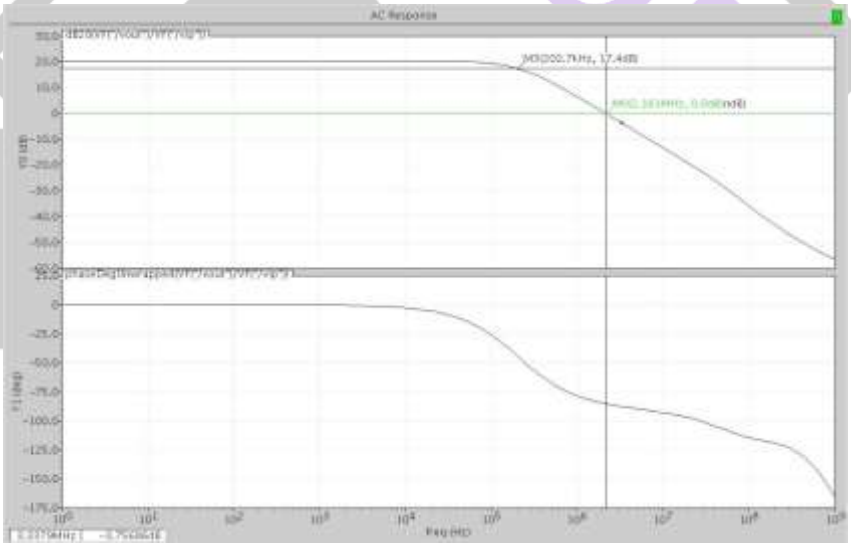


Figure 7: Op-Amp bandwidth

LAYOUTS AND RC –EXTRACTED VIEWS

Bias circuit for amplifier current sinks:

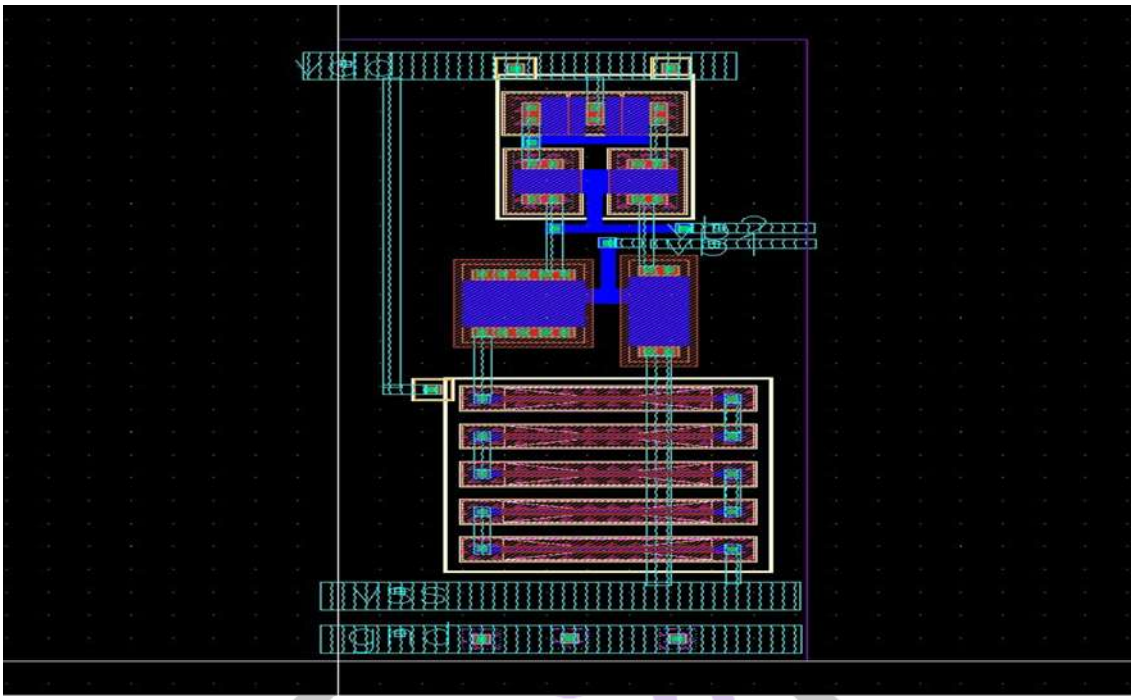


Figure 8: Op-Amp RC extracted view

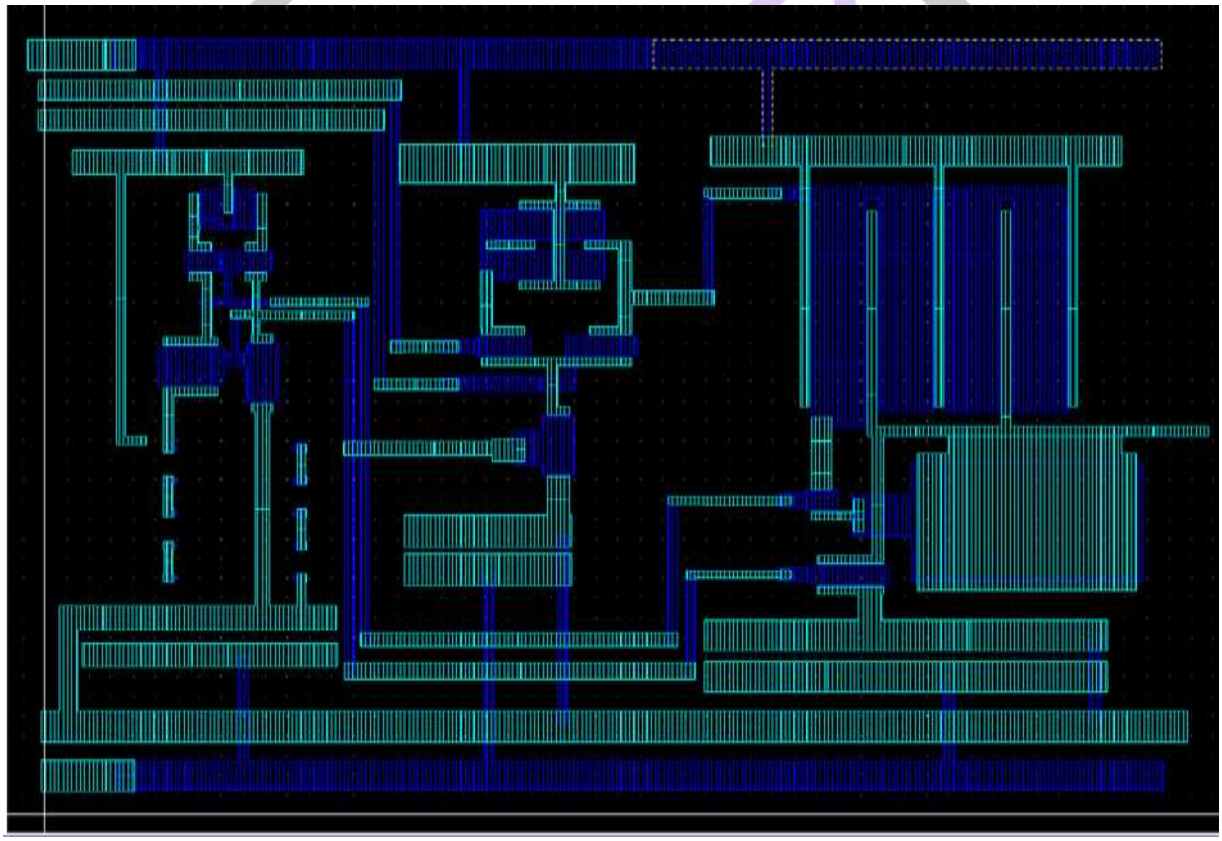


Figure 9: Op-Amp RC extracted view

VIII.CONCLUSION

The proposed design has been able to satisfy most of the specifications provided for the op-amp. The proposed op-amp is a two stage single output op-amp. The input stage is a differentialamplifier and a common source stage forms the second stage of the op-amp. The layout of thedesign has been made and simulated. The post layout simulations abide by the given specification. The entire design has been done in UMC 180 nm technology. The gain of the op-amp can be increased further by the use of cascade device in the input stageThe voltage swing may be increased by using a double ended output.

Table 1: Observations for low power op-amp with supply 1.8v

Parameters	Specification	Simulation Results before layout	Simulation Results after layout
Gain	10 V/V || 20 Db	12 V/V || 22 dB	10.2 V/V || 20.14 dB
3-dB Bandwidth	20 kHz.	397 kHz.	200 kHz
UGB	N/A	4.6MHz	2.165 MHz
CMRR	>50 dB	80dB	64dB
PSRR	N/A	84dB|59dB	87dB|60dB
SLEW RATE	10 v/µs	25 v/µs	12.47v/µs
POWER DISSIPATION	1 mW.	0.9 mW	0.6 Mw
Output Offset Voltage	N/A	-600 mV	-600 Mv

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