Design Model of Retiming Multiplier for FIR Filter and its Verification

[1]DONDA KATYAYANI, [2]PRADEEP KONDAPALLI

[1]P.G Scholar, [2]Associate Professor
Baba Institute of Technology & Sciences,
Visakhapatnam, Andhra Pradesh

***Abstract*: In recent years in VLSI technologies Multiplication operation cause great rating Digital type filters. The main objective is to increase the speed and reduce the delay as well as power consumption. Low and reduced power consumption with better performance, Architecture based on the retaining multiplier for finite impulse response. The design of a low-voltage micropower asynchronous (async) signed truncated multiplier based on a shift–add structure for power-critical applications such as the low-clock-rate (4 MHz) hearing aids is described. The emphases of the design are micropower operation and small IC area, and these attributes are achieved in several ways. An error correction methodology is proposed to mitigate, where appropriate, the arising truncation errors. The errors arising from truncation and the effectiveness of the error correction are analytically derived. Third, a low-power shifter design and an internal latch adder are adopted. Finally, a power-efficient speculative delay line is proposed to time the async operation of the various circuit modules. A comparison with competing synchronous and async designs shows that the proposed design features the lowest power dissipation (5.86 W at 1.1 V and 1 MHz) and a very competitive IC area (0.08 mm using a 0.35- m CMOS process). The application of the proposed multiplier for realizing a digital filter for a hearing aid is given.**

Index Terms: Asynchronous (async) circuits, finite-impulse response (FIR) filter, low power, shift–add multiplier

I.INTRODUCTION

The importance of DSP systems with low power, low area and high performance appear to be increasing with no visible sign of saturation. Digital filters play a vital role in digital systems where Finite Impulse Response (FIR) filters are one of the most widely used fundamental devices. The topology of the multiplier circuit also affects the resultant power consumption. Choosing multipliers with more hardware breadth rather than depth would not only reduce the delay, but also the total power consumption. Therefore by reviewing all the above mentioned papers, the low power multiplexer based on shift/add multiplier without clock pulse for reduce dynamic power consumption of a digital FIR filter is a better solution to reduce power. D flip flop is used for delay operation by retaining its stable input registered value. And also pipelining is better topology to minimize the total time taken for the design and also gives high performance. Therefore in our implementation we are using FIR filter design, based on Low Power Multiplexer Base Shift/Add multiplier. And also appropriate adder is chosen which consumes less power and effective performance to increase the speed. Till now, from the adders‟ survey we found that Carry look ahead and carry select adders are designed for higher performance. Once the implementation of this FIR filter is completed, this filter is compared with other common implementations for area and power.

II. LITERATURE SURVEY

FIR filters are the main computational part of the DSP systems for signal processing. Digital FIR filter design for low power concept has become vast applied technique now days and there are so many proposed research architectures for this low power concept [1], [2], and [4]. There also proposed research architectures for higher performance and low power design [3] and [5]. One of the implementation includes Latch based and pipelining techniques for 6 Tap FIR filter to achieve Low power. The power reduction is achieved through the usage of a MAC unit inside the filters that reduce the total activity and therefore the dynamic power. Digital FIR filter is given with finite state machine input values and filter coefficients. 1-bit MAC unit is designed with enable to reduce the total power consumption. They used MATLAB for filters design and VHDL code for synthesis operation. Active-HDL and Altera Quartus II used for simulation and functional verification is carried out simultaneously. It is seen that Latch based design can reduce the dynamic power consumption [1].

Clock gating and pipelining techniques are used to design and implement FIR filters to achieve low power. MAC unit is the major part of the FIR filter and in the majority of digital signal processing (DSP) applications the critical operations are the multiplication and accumulation. Multiplier-Accumulator (MAC) unit that consumes low power is always a key to achieve a high performance digital signal processing system. For arithmetic circuits, a large portion of the dynamic power is wasted on un-productive signal glitches. By using pipelining and block reordering methods one can reduce the glitches in the circuits in turn reduce the power consumption. D flip flop is used for clock gating operation [2]. FIR filter is used in many DSP applications and many other synthesis operations of signal require large order FIR filters. The multiplier here they used is Vedic Multiplier. It will reduce the number of partial products generated by a factor of 2. The carry save adder is used in place of adder to avoid the unwanted addition and thus minimize the switching power dissipation. Here they designed FIR filter for 8bit adders and 8bit multiplier and are achieved via VHDL hardware description language using Xilinx ISE software synthesized and implemented on FPGA in Virtex IV family. Also power is analyzed using Xilinx XPower analyzer.

The above proposed optimization techniques reduce the power dissipation in the digital FIR filter [3]. Signal processing in wireless sensor network has a vast range of applications. This [4] reviews several techniques used for designing & implementing low power digital filters for wireless sensor network (WSN). Here they proposed some techniques such as Modified Booth Encoding Algorithm combined with Spurious Power Suppression Technique, Low Power Digit Serial Multiplier along with carry look ahead adder, shift/add multipliers etc. These techniques are used to achieve low power consumption in VLSI-DSP applications, from algorithm and architectural levels to logic, circuits and device levels to reduce power consumption. Another important comparative analysis of Parallel FIR filter [5] deal with the design and implementation of parallel FIR filter structure on FPGA using 4 different parallel processing methodologies with minimal cost of hardware. This deals with the comparative performance analysis of traditional parallel FIR filter with respect to the FFA (Fast FIR Algorithm), transposition and symmetric convolution based parallel FIR filter. By Comparison result they showed that FFA and symmetric convolution based structures save significant number of multipliers with an expense of additional adders and exploits the hardware complexity incurred by the traditional structure.

III. Multiplier based FIR FILTER

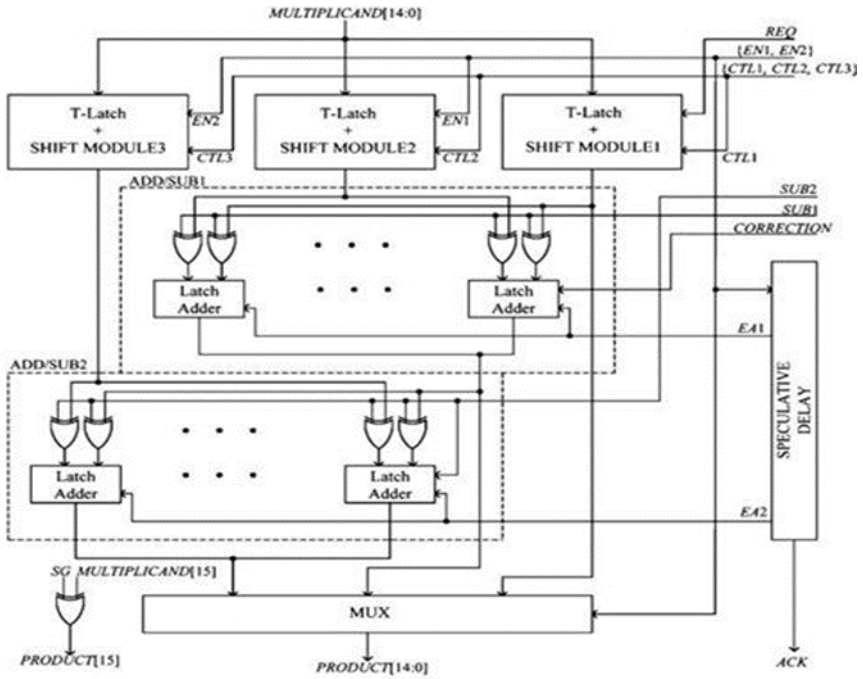

Fig. 1. Architecture of the proposed async shift–add multiplier.

Fig. 1 shows the circuit block diagram of the proposed multiplier with a maximum of three SPT terms. The inputs are the multiplicand operands, and the control signals are REQ (Request—to initiate multiplication), EN1 (Enable1—the second SPT term exists, thereby enabling the processing of the second SPT term), EN2 (Enable2—the third SPT term exists, thereby enabling the processing of the third SPT term), CTL1 (Control1—to control the shift operation of SHIFT MODULE1), CTL2 (Control2—to control the shift operation of SHIFT MODULE2), CTL3 (Control3—to control the shift operation of SHIFT MODULE3), SUB1 (Subtract1—the second SPT term is negative, thereby performing subtraction operation in ADD/SUB1), SUB2 (Subtract2—the third SPT term is negative, thereby performing subtraction operation in ADD/SUB2), CORRECTION (see later), and SG (the sign bit). The outputs are PRODUCT [15:0] and ACK (Acknowledge—to indicate the completion of multiplication). Note that, because the multiplier operand can be predecoded and stored directly as control signals (rather than actual 16-bit coefficients in memory), a decoding circuit hardware is not required. This approach results in simpler hardware as there is no need to convert the coefficients to control signals.

The async approach is adopted in the multiplier primarily for control simplicity and for low power dissipation. These are attributed to two reasons. First, the async circuit is essentially a self-timed circuit with inherent timing control. By means of our earlier proposed LAs [13], [14] and the async operation, the LAs therein are controlled adaptively (for four different cases) by a novel speculative delay line (see later) to control the async multiplier asynchronously. Note that no additional latch (as a separate circuit element) is required to latch the intermediate results, hence resulting in low hardware overhead and low power dissipation. Second, fine-grain gating is innate in async circuits. By means of async operation, the proposed multiplier operates such that only the modules that are necessary during the multiplication process are enabled and the remaining modules are disabled, thereby blocking unnecessary switching. In this fashion, power dissipation is reduced and also partly because glitch/spurious switching is virtually eliminate.

The operation of the proposed multiplier will now be described with some emphasis on the pertinent design approaches adopted to reduce power dissipation. When the REQ is asserted to initialize a multiplication process, the T-Latch will first synchronize the multiplicand operand (see Fig. 4) to the three shift modules, and each module handles one SPT term. The SPT

terms are weighted more heavily from Shift Module 1 to Shift Module 3. As it is known that Shift Module 1 always generates an output greater than Shift Modules 2 and 3, subtraction can be performed without the need for magnitude comparison—the circuit path can hence be simple and the power dissipation low. Put simply, a comparator is not required for the SM subtraction and the probability of a high degree of switching in the proposed design is low. When the multiplication process is complete, the ACK signal will be generated.

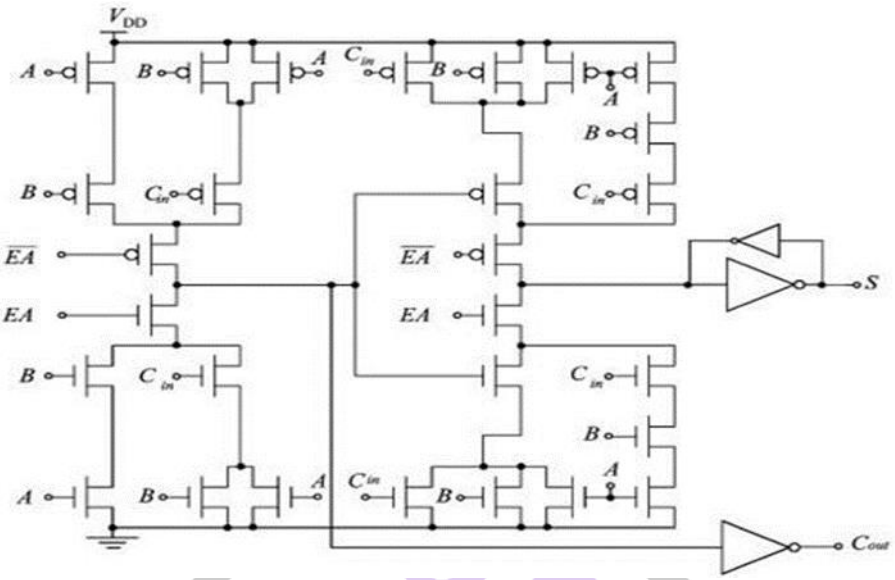

Fig 2: Proposed Latch Adder.

Our LAs [without the weak inverter in the carry-out signal as shown in Fig. 2 [13], [14] are employed, resulting in lower power dissipation than a conventional design. This is because only the Sum signal needs to be connected to the next module; hence, the weak inverter is only required in the Sum signal to latch the data (when the signal is inactivated). As speed is not a critical parameter (4-MHz clock rate), small transistor aspect ratios in the LAs are selected, to keep the load capacitances small. These LAs are timed and enabled after a certain delay determined from the delay line associated with the LAs. This is to reduce spurious switching due to the poorly synchronized outputs from the different shift modules to the ADD/SUB modules.

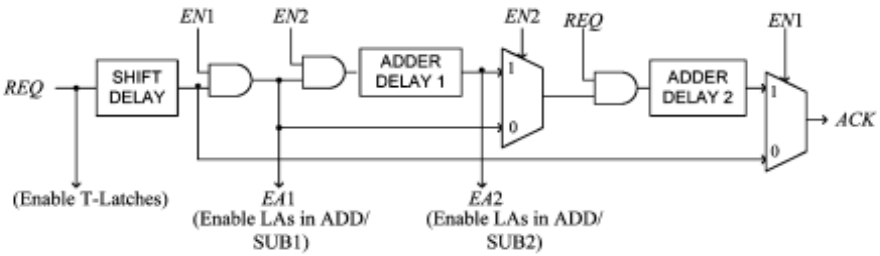

Fig 3: Proposed speculative delay line.

IV. SIMULATION RESULTS

The proposed async shift–add based retiming multiplier is verified by means of HSPICE and NANOSIM computer simulations at 1.1 V and 1 MHz and on the basis of measurements on a prototype IC embodying the proposed multiplier. The microphotograph of the prototype IC is shown in Fig. 4.

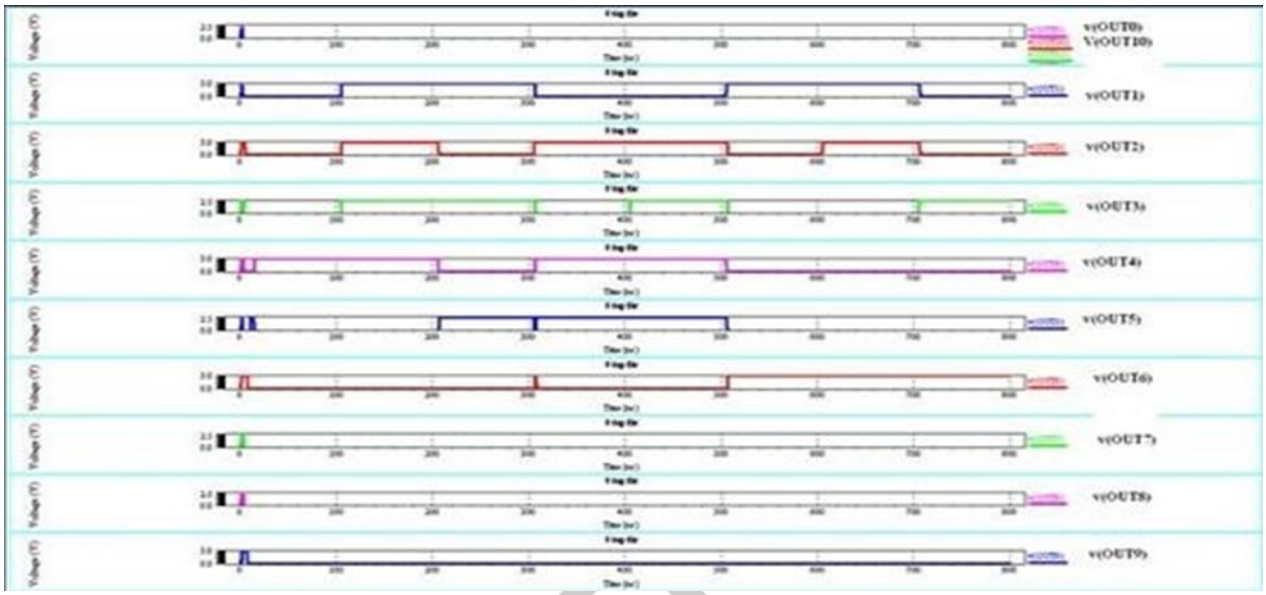

Fig 4: Output Waveform for Proposed Multiplier

Table 1: Performance Analysis of Asynchronous Multiplier Based Filter Design

Parameter	FIR Filter based Multiplier			Proposed FIR Filter based Multiplier		
No.of Taps	4	8	16	4	8	16
Power Dissipation (mW)	8.42	17.1	29.51	6.14	12.5	21.85
Average Delay (ns)	0.71	0.75	0.79	0.71	0.73	0.77
Power Delay Product (pJ)	5.98	12.83	23.31	4.35	9.13	16.17

V. CONCLUSION

In the last research work, a comparison of different FIR filter designs as discussed above has been done. On comparing the results obtained from the above discussion, it is found that the XOR-XNOR based DA FIR filter shows less power dissipation as well as less power delay product when compared to other proposed FIR filter designs. By comparing the power delay product among the proposed methods for the design of FIR filter, it is evident that the XOR-XNOR based DA FIR filter outperforms the other proposed designs. XOR-XNOR based FIR filter is also better in power delay product when compared to those of the other researcher's proposed FIR filter design. To reduce the power dissipation, a number of low-power techniques at the system level (SM data and the sum of SPT terms representation) and low-power circuit design methodologies have been proposed and adopted. The quantization error arising from the truncation and with the limited number of SPT terms has been quantized, and an error-correction scheme to mitigate this error has been proposed. It has been shown that the proposed design depicts the lowest power dissipation compared with reported designs and that its IC area requirement is very competitive.

REFERENCES

[1] B.-H. Gwee, J. S. Chang, and H. Y. Li, "A micropower low-distortion digital pulse width modulator for a digital Class D amplifier," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 49, no. 4, pp. 245–256, Apr. 2002.
[2] W. Shu and J. S. Chang, "THD of closed-loop analog PWM Class D amplifier," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 6, pp. 1769–1777, Jul. 2008.
[3] T. Ge and J. S. Chang, "Modeling and technique to improve PSRR and PS-IMD in analog PWM Class D amplifiers," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 55, no. 6, pp. 512–516, Jun. 2008.
[4] K.-S. Chong, B.-H. Gwee, and J. S. Chang, "Energy-efficient synchronous-logic and asynchronous-logic FFT/IFFT processors," IEEE J. Solid-State Circuits, vol. 42, no. 9, pp. 2034–2045, Sep. 2007.
[5] Y. W. Li, G. Patounakis, K. L. Shepard, and S. M. Nowick, "High-throughput asynchronous datapath with software-controlled voltage scaling," IEEE J. Solid-State Circuits, vol. 39, no. 4, pp. 704–708, Apr. 2004.
[6] H. H. Dam, A. Cantoni, K. L. Teo, and S. Nordholm, "FIR variable digital filter with signed power-of-two coefficients," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 54, no. 6, pp. 1348–1357, Jun. 2007.
[7] Z. Tang, J. Zhang, and H. Min, "A high-speed, programmable, CSD coefficients FIR filter," IEEE Trans. Consum. Electron., vol. 48, no. 4, pp. 834–837, Nov. 2002.
[8] M. J. Wirthlin, "Constant coefficient multiplication using look-up tables," J. VLSI Signal Process. Syst., vol. 36, no. 1, pp. 7–15, Jan. 2004.
[9] L. S. Nielsen and J. Sparsø, "Designing asynchronous circuits for lowpower: An IFIR filter bank for a digital hearing aid," Proc. IEEE, vol. 87, no. 2, pp. 268–281, Feb. 1999. [10] C. C. Chua, B.-H. Gwee, and J. S. Chang, "A low-voltage micropower

asynchronous multiplier for a multiplierless FIR filter," in Proc. IEEE Int. Symp. Circuits Syst., Bangkok, Thailand, 2003, vol. 5, pp. 381–384.
[11] A. P. Chandrakasan, "Ultra low power digital signal processing," in Proc. 9th Int. Conf. VLSI Des., 1995, pp. 352–357.