Design and Implementation of Digital Circuits in LFSR using Test Pattern Generation

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***Abstract*: The external testing of VLSI circuits is old, complex and time consuming. The external testing VLSI circuits is also costly. The Built-in Self-Test is a new technology, applied to the VLSI circuits to test condition of the circuits. The BIST structure consist of four major components such as test patter generator, circuit under test, output response analyser and BIST controller. The Linear Feedback Shift Register (LFSR) is the major component of test pattern generator. LFSR is acting as test pattern generator in most of the BIST structure. The output of the test pattern generation is applied as input to circuit under test. The output of the circuit under test is applied to the output response analyser. The outputs for the corresponding test vector is already stored in the output response analyser. The stored output and the output of the circuit under test are same then the circuit is claimed as fault free, otherwise the circuit has some fault. Three LFSR based test pattern algorithms are developed for the three circuit under test in the proposed research work. The three circuits we considered for the circuit under test are the benchmark circuit's c432, s27 and c17.**

***Keywords*: LFSR, BIST, c432, s27, c17**

I INTRODUCTION

Design for Testing (DFT) and Built In Self-Test (BIST) are the methods to test the chip at the design phases for 100 percent stuck-at-fault. DFT has several methods to increase controllability and observability such as scan design method, on chip hardware for test pattern generation and data compression methods. Various methods of DFT is combined to form BIST scheme. The important BIST schemes are combined test pattern generation, built in evaluation, self-test, partitioning, multiplexer test point insertion, serial scan and random test pattern.

The test patterns are generally generated to test the chip at three different levels. They are application level, functional level and structure level. The application level of test pattern generation is done by customer. The customer can generate pattern to test the chip. This application level test pattern generation may not guarantee to be 100 percent defect free. The function level test pattern generation used to test at subunits, modules and black boxes level. In this the input patterns are tested with the output pattern.

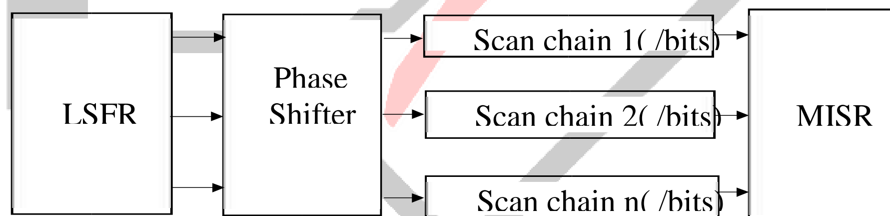

Figure: 1 BIST architecture with LFSR

The BIST architecture using Linear Feedback Shift Register (LFSR) is shown in Figure 1. The time shifting and repeating operation is to be done on the outputs of linear feedback shift register. The LFSR and phase shift registers increases the effectiveness of fault detection. The phase shift register is designed by XOR gates. The output of the circuit under test will compacted by multiple input shift register. The output of the CUT will be compared with fault free signature to test the circuit.

The test pattern generator is shown in Figure 2. The test patterns are generated and sent to the fault less VLSI chip and actual VLSI chip of same architecture. The outputs of fault less VLSI chip is compared with actual VLSI chip by EXOR gate. The EXOR gate produce low output if there is no fault. It produce high output when there is difference between the outputs of two VLSI chip and means the actual VLSI chip is faulty one

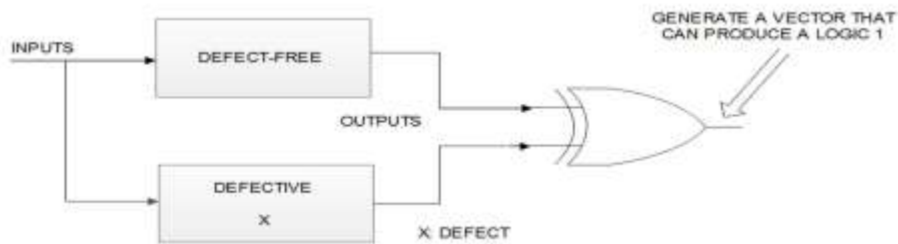

Figure: 2 Test pattern generation

Automatic test pattern generators are available to generate test patterns. Minimum number of test pattern with large fault coverage is more advantageous. The stuck-at fault is one of the most common fault normally occur in the digital logic circuits. Random test pattern generation technique is available for test pattern generation.

II LITERATURE REVIEW

Rinitha & Ponni (2016) described functional testing. It is a testing of internal structure of a program. Certain specific inputs are given and corresponding outputs are tested. In this way the functionality of software is tested. It is different from the system test. In functionality test the data base, client server application and security tests are carried out. There are many types of functional test. The functional test includes integration testing, unit testing, system testing, sanity, smoke testing and regression testing, black box testing and acceptance testing (Rinitha & Ponni 2016).

Bardell *et al*. presented Built-in Test for VLSI. It is scan based structural testing. It tests the flip-flops, latches and combinational logic circuits by supplying known input pattern and output pattern. If there is a mismatch in pattern, then that particular device is fault. The speed at the input pattern supplied is taken for the generation of output is also tested with respect to the frequency of the device. In scan delay test a pair of vector is used to test paths and connections of the circuits at the specified speed (Rinitha & Ponni 2016).

Rinitha & Ponni (2016) also explained the concept of built in selftest. The built in self-test is explained with the help of circuit diagram as shown in Figure 3. It is a Built in self-test is a test of checking the functionality of chip hardware, board and finally the system also.

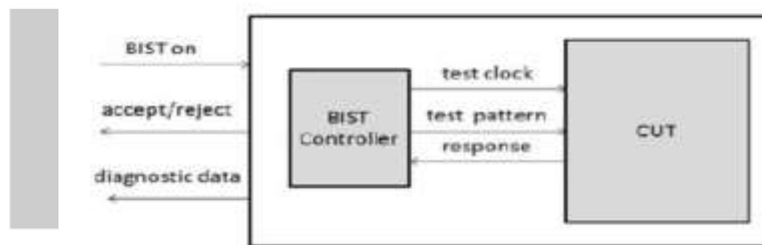

Figure: 3 Built in self-test

Trupti Patil & Amol Dhankar (2016) proposed a new test pattern generation to reduce the power consumption in VLSI circuits during testing. A low power BIST was designed using a feedback shift register. This architecture is constructed using VHDL as a software tool (Trupti Patil & Amol Dhankar 2016). The low power LFSR is shown in figure 4. In the low power circuits the disabled flip flop will not consume any power at the same time it will not alter the circuit conditions.

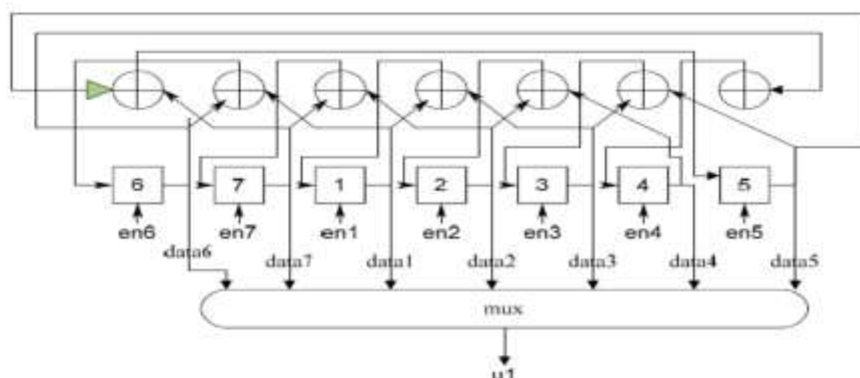

Figure: 4 Low power LFSR structure

The memory element consumes less power when not in use. In this structure the number of switching activities are reduced in order to reduce power loss (Trupti Patil & Amol Dhankar 2016). Only one flip flop is enabled during every shift operation in the LFSR in low power LFSR structure. The feedback is also made smaller as much as possible to reduce the power consumption (Trupti Patil & Amol Dhankar 2016). This low power structure is designed by HDL tool.

III IMPLEMENTATION

3.1 LFSR BASED TEST PATTERN GENERATION FOR BENCHMARK CIRCUIT c432

Several VLSI manufacturing companies used benchmark circuits to test their products. They normally used two categories of circuits, one is combinational circuits and another one is the sequential circuit. The most commonly used combinational circuit is ISCAS-85. Similarly the most commonly used sequential circuit is ISCAS-89. These circuits are used to implement the BIST. These benchmark circuits are mainly used for the purpose of testing the test pattern generation (Lakshmi Divya, Praveen Kumar, 2014). One of the ISCAS-85 circuits is c432 to the test pattern generation. The bench mark circuit c432 is a 27 channel interrupt controller.

The inputs for this interrupt controller are three 9 bits busses. These busses are named as Bus A, Bus B and Bus C. Another 9bit bus is there to enable or disable the interrupt request. Totally the bench mark c432 has 36 input lines. The combinational benchmark circuit c432 is shown in Figure 5.

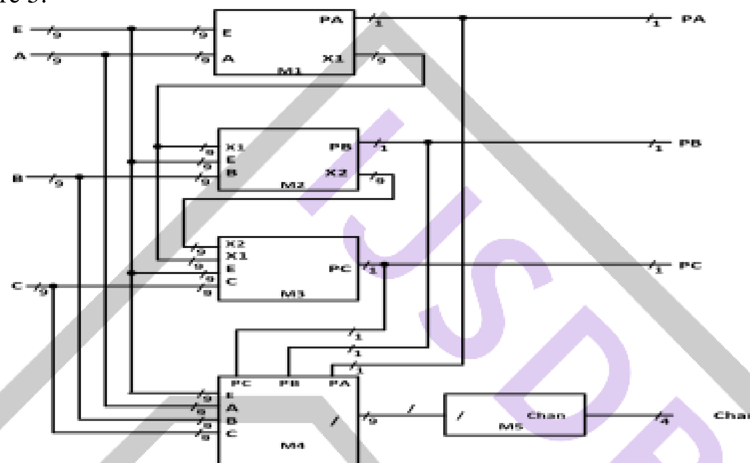

Figure: 5 Combinational bench mark circuit c432

c432 has seven output lines. The c432 benchmark circuit is designed with 160 logic gates. The priority of the interrupt request is decided by the internal bit positons. The 27 channel interrupt controller is designed in terms of five modules. The five modules are named as M1, M2, M3, M4 and M5. The issues to be analysed are fault coverage, test time, hardware overhead, and optimal design. The 27 channel interrupt controller generates seven numbers of outputs.

3.2 LFSR BASED TEST PATTERN GENERATION FOR BENCHMARK CIRCUIT s27

Benchmark circuits are used to test the various combinational and sequential circuits to test their performance. The most commonly used combinational circuit in ISCAS-85 are c432, c499, c880, c1355, c1908, c2670, c3540, c5315, c6288 and c7552. Several VLSI manufacturing companies used benchmark circuits to test their products. They normally used two categories of circuits, one is combinational circuits and another is the sequential circuit. Similarly the most commonly used sequential circuits are ISCAS-89. They are s27, s208, s298, s344, s349, s382, s386, s400, s420, s444, s499, s510, s526, s635, s641, s713, s820, s832, s838, s938, s953, s967, s991, s1196, s1238, s1269, s1423, s1488, s1494, s1512, s3271, s3330, s3384, s4863, s5378, s6669, s9234, s13207, s15850, s35932, s38417 and s38584. These circuits are used to implement the BIST. These benchmark circuits are mainly used for the purpose of testing the test pattern generation (Lakshmi Divya, Praveen Kumar, 2014). One of the ISCAS-89 circuits is s27 to the test pattern generation. The sequential bench mark circuit s27 is shown in Figure 6.

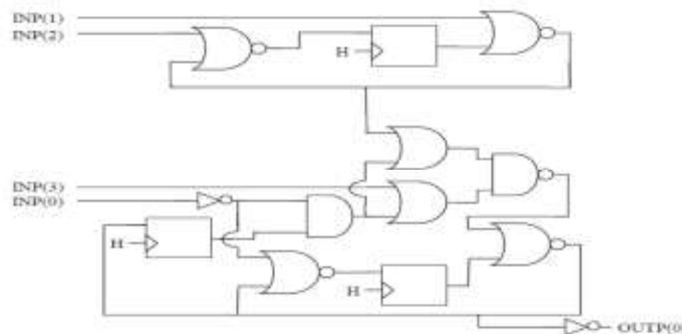

Figure: 6 Sequential bench mark circuit s27

The sequential benchmark circuit consists of D flip flops and logic gates like NNAD, AND, OR, NOR and NOT gates. There are 3 numbers of D flip flops, one number of NAND gate, one number of AND gate, two numbers of OR gates, four numbers of NOR gates and two numbers of NOT gates. The s27 circuit is a scan circuit and takes four inputs to produce one output. The s27 circuit is designed using thirteen numbers of logic gates and flip flops. The connections of the input signals and output signal is clearly shown in Figure 6.

3.3 LFSR BASED TEST PATTERN GENERATION FOR BENCHMARK CIRCUIT c17

There are many benchmark circuits are developed to test the performance of the developed test pattern generation techniques. Many benchmark circuit are developed in ISCAS-85 and ISCAS-89. The benchmark circuit c17 has five inputs namely a, b,c,d and e and it produces two outputs namely F and G as shown in Figure 7.

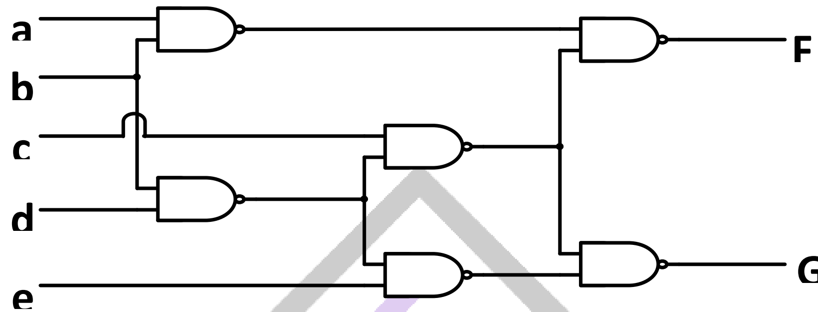

Figure 7. Combinational bench mark circuit c17

The combinational benchmark circuit c17 is designed by using only NAND gates. There are six NAND gates are used to develop the benchmark circuit c17. Five inputs are applied to four NAND gates as shown in Figure 5.2. The outputs are received from two of the NAND gates available at the end of the circuit as shown in Figure 5.2. The benchmark circuit c17 will receive inputs from the LFSR and produce outputs. The outputs are tested with the comparator. The comparator will check the output of the benchmark circuit with the values stores in the memory. If there is any deviation then the circuit is claimed as faulty one otherwise the circuit is fault free circuit.

IV. SIMULATION RESULTS

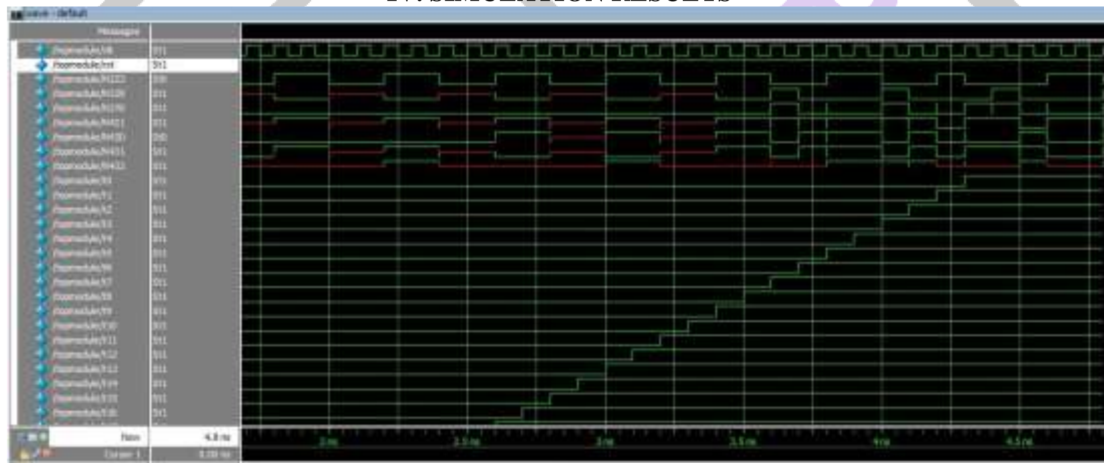

Figure 6.10 Output waveform of Benchmark circuit C432 without fault

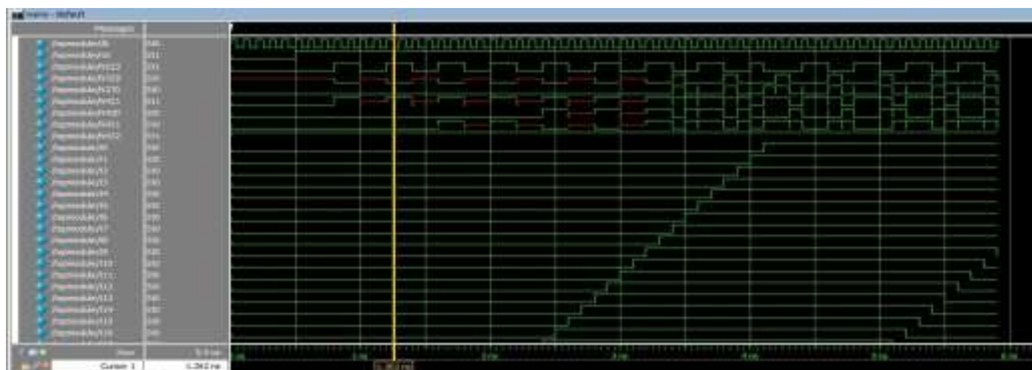

Figure 6.12 Output waveform of Benchmark circuit C432 with fault

Figure 6.19 Output waveform of Benchmark circuit s27 without fault

Figure 6.21 Output waveform of Benchmark circuit s27 with fault

Figure 6.27 output waveform of Benchmark circuit c17 without fault

Figure 6.29 Output waveform of Benchmark circuit c17 with fault

Table 6.12 Devices utilization summary for Different Bench mark circuits

Devices	c432		s27		c17	
	without fault	with fault	without fault	without fault	without fault	with fault
Slices	68	71	23	3	3	3
Flip Flops	36	36	34	5	5	5
4 input LUTs	92	98	31	1	4	4
IOs	9	9	7	7	4	4
Bonded IOBs	9	9	7	7	4	4
GCLKs	1	1	2	1	1	1

Table 7.3 Comparison of execution time

Circuit	Execution time in ns	
	Without fault	With fault
c432	28.7	37.94
s27	4.462	4.95
c17	5.899	5.907

Table 7.5 Comparison of Power consumption

Circuit	Power consumption in milli Watts	
	Without fault	With fault
c432	280.68	298.15
s27	261.74	276.3
c17	253	260.29

V.CONCLUSION

Three LFSR based test pattern generation algorithms are developed to test the digital circuits. There are three benchmark circuits such as c432, s27 and c17 are considered as circuit under test. The Xilinx ISE 8.2 is used to develop program. The coding for the LFSR and circuit under test are developed in Xilinx programming. The LFSR based test pattern generation for the benchmark circuit c432 is developed in Xilinx ISE 14.7. In testing c432, 50 faults are created to test the performance the circuit under test, all the 50 number of faults are detected by the proposed algorithm and its fault coverage is 100.00%. The execution time, memory usage and power consumption obtained by the proposed test pattern generation algorithm under fault free condition for the benchmark circuit c432 are 27.8ns, 170884KB and 280.68mW respectively. The execution time, memory usage and power consumption obtained by the proposed test pattern generation algorithm under fault condition for the benchmark circuit c432 are 37.94ns, 169668KB and 298.15mW respectively. The execution time, memory usage and power consumption obtained by the proposed test pattern generation algorithm under fault condition for the benchmark circuit s27 are 4.952ns, 194220KB and 276.3mW respectively. The execution time, memory usage and power consumption obtained by the proposed test pattern generation algorithm under fault condition for the benchmark circuit c17 are 5.907ns, 192068KB, 260.29mW respectively.

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