Design of Low Power RRAM Cell Using CNFET

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Abstract: **This Project presents a CNFET based novel RRAM cell using memristor as memory element. The proposed RRAM cell is designed in such a way that half-select issue is resolved. Simulation results of critical design metrics of the proposed RRAM cell and previous 2T2M RRAM cell are compared. The proposed RRAM cell achieves 6.13× lower read delay along with 33× lower hold power due to use of MTCMOS power reduction technique than 2T2M cell at nominal VDD. It is a half-select free non-volatile RRAM cell with faster read operation and it is also power efficient.**

Keywords**: Memristor; RRAM; non-volatile; CNFET; read delay; write delay**

I. INTRODUCTION

Further, according to Moore's law, the number of transistors that can be manufactured on a single chip is expected to grow exponentially with time [5]. This prediction turned out to be true as illustrated in Figure 1.1 [6-7]. Figure 1.1 plots the decrement in number of transistors integrated on a single microprocessor chip as a function of time. As can be observed, integration density doubles in every 18 months. To meet the IC density predicted by Moore's law, technology scaling has been pursued aggressively until today since 1970s. The gate length of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is scaled down by a factor of 0.7 in every 2 years, as shown in Figure 1.1. Since 2006, at 65 nm technology node the gate length of a MOSFET has arrived at deep sub- micron/nano range. Today, technology node is 20 nm, and 14 nm has been expected as feature size in the near future [7-8].

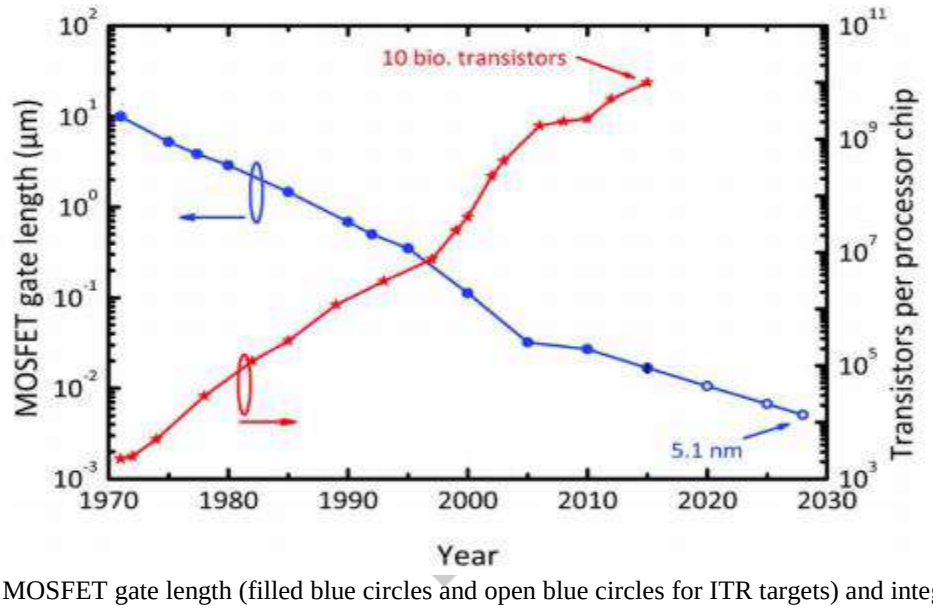

Figure: 1 Evolution of MOSFET gate length (filled blue circles and open blue circles for ITR targets) and integration complexity of microprocessor chip (red stars), as a function of time

Researchers developed double-gate MOSFETs and FinFET/tri-gate devices [14-15] to reduce short channel effects. In these devices, gate is placed on two/three sides of the channel, which results in better control on the channel and considerable reduction in drain to source sub-threshold leakage current. Researchers also have begun the exploration of new devices and channel material in sub10 nm technology node, which could be the possible alternatives to Si-CMOS. Based on ITRS [16], some of the emerging devices which have the capabilities to replace Sitechnology in post Si era are nanowire field effect transistor (NWFET) [17], III-V compound semiconductor field effect transistor [18-21], graphene field effect transistor [22-24], and carbon nanotube field effect transistor (CNTFET) [25-27].

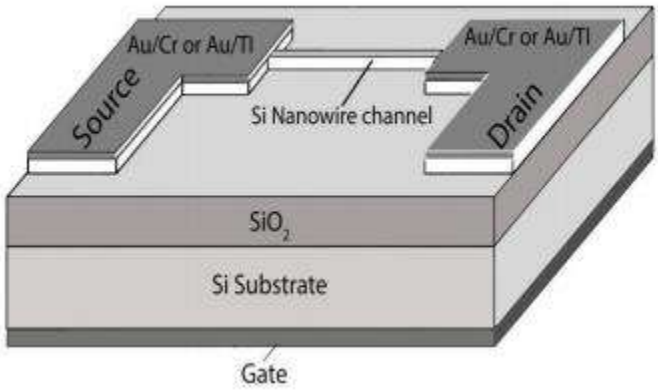

Figure 2: Schematic view of Si based NWFET

CNTFET uses a single or an array of semiconducting single wall carbon nanotubes (SWCNTs) as a channel material. The gate electrode is placed above the CNT channel and separated from it by a thin layer of gate dielectric. The schematic view of CNTFET is shown in Figure 1.5, where an array of four SWCNTs is used for channel [39]. CNTFET could be more achievable and promising candidate to extend or complement traditional Si device due to its excellent properties such as ballistic transport operation [40], high carrier mobility (103 -104 cm 2 /V-S) [41], easy integration of high-k dielectric material [42] (other than SiO2) resulting in better gate electrostatics, strong chemical bonding, high thermal conductivity (1700-3000 W/mK), high chemical stability [41], and better matching of P and N-type CNTFETs which simplifies transistor sizing in complex circuits.

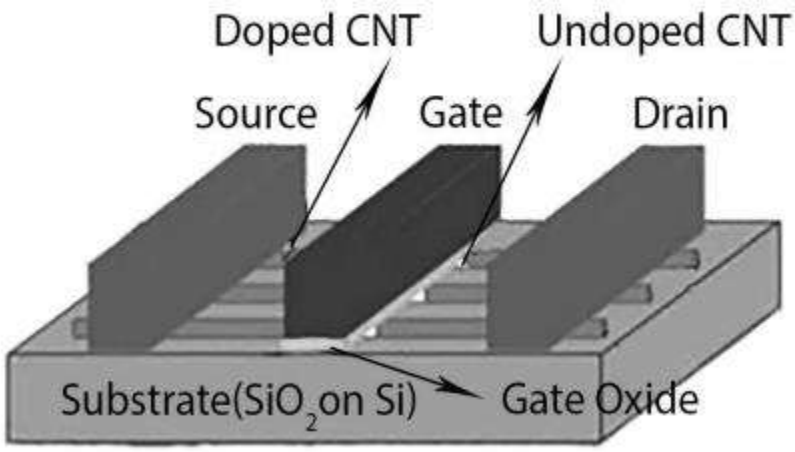

Figure 3: Schematic view of CNTFET

II. BACKGROUND AND RELATED WORK

This chapter provides an overview of ternary logic and CNFETs. A brief review of existing CNFET-based implementations of ternary logic circuits is also presented in this chapter.

2.1 TERNARY LOGIC:

Binary logic, when given a significant third value is called ternary logic or three valued logic and functions realized with three values are called ternary logic functions. The values 0, 1 and 2 form the nomenclature to denote the ternary values in this work. A function $f(X)$ is defined as a ternary logic function mapping {0, 1, 2} n to {0, 1, 2} where X is given by $X1,....,Xn$. When}, the basic operations of ternary logic can be defined as:

$$Xi + Xj = max\{Xi,Xj\} \quad (2.1)$$

$$Xi \cdot Xj = min\{Xi,Xj\} \quad (2.2)$$

Where equations (2.1) and (2.2) indicate OR and AND operations respectively for ternary logic [36]. Another important logic function in ternary logic is a ternary inverter.

2.2 Single-Walled Carbon Nanotube (SWCNT):

A single-walled carbon nanotube (SWCNT) is obtained by rolling up a sheet of graphite along a roll-up vector $C = na+mb$, as shown in Figure 2.1, where m and n are positive integers which specify the chirality of the tube and $0a0$ and $0b0$ are lattice unit vectors [42]. The angle of atom arrangement along the tube, also called as chiral angle or roll-up vector or chirality vector in a single wall CNT (SWCNT), is represented by an integer pair (n,m). The value of (n,m) determines if CNT is metallic or semiconducting.

SWCNT is further classified into three groups, depending on the angle of atom arrangement, i.e. chirality vector, along which the CNT is rolled. The three groups of CNT are named as armchair CNT if CNT has $n = m$, zigzag CNT if $n = 0$ or $m = 0$ and chiral

CNT if *m* and *n* are different and nonzero. All armchair CNTs behave as conductors. On the other hand, zigzag and chiral CNTs show metallic (conducting) behavior when $n = m$ or $n–m = 3i$, where i is an integer, otherwise they show semiconducting behavior. Hence zigzag and chiral CNTs are used in realizing a CNTFET [43]. The chirality vector (*n*,*m*) also sets the diameter of the CNT.

Carbon-Nanotube Field Effect Transistor (CNFET) is a transistor which makes use of semiconducting carbon nanotubes as channel material between two metal electrodes that act as source and drain contacts. The operating principle of CNFET is similar to that of MOS transistors. As shown in Figure 2.2, this three (or four) terminal device consists of a semiconducting nanotube, acting as conducting channel, bridging the source and drain contacts. The device is turned on or off electrostatically via the gate. The drain current is directly proportional to the number of CNTs connected between the source and the drain and their respective diameters [44,45]. Three types of CNTFET devices have been reported in the literature. They are known as schottky barrier CNTFET (SB-CNTFET), MOSFET-like CNTFET (MCNTFET) and band-to-band tunneling CNTFET (T-CNTFET).

III. DESIGN OF RRAM USING CNFET

This section gives a brief description about structure and working of the proposed 2CNFET-2M RRAM cell. In the proposed cell as shown in Fig. 4.1, two CNFETs are connected in series to access the data line DL and the storage node is connected to two memristor connected in opposite polarity to each other. NCNFET1 is controlled by a row word line and NCNFET2 is controlled by a column word line and this arrangement helps in resolving the half select issue which will be discussed later in this section. The problem with cells consisting of single memristor is that such cells are not dependable and have issues with process variations. These problems can be overcome by using two memristor which make it a differential structure. The cell is active only when both the column and read word lines are active thus eliminating the issue of a cell being half selected. Also with the use of CNFETS, speed and power consumption of the cell is improved.

A. Write Operation

Activating row word line and column word line marks the beginning of write operation. Both RWL and CWL should be turned on to write data to the storage node. According to the data that has to be written data line is pre-charged or pulled down to the ground and quite opposite is the case with BL and BLB. If '1' has to be written on to the storage node data line (DL) is pulled up to and BL and BLB both are pulled down to ground. During write-1 operation two CNFETs in series pass '1' from data line DL to the storage node 'g' and now out of the two memristors connected in opposite polarity one will go to low resistance state and the other will go to high resistance state because node g is at a bit higher voltage than BL and BLB.

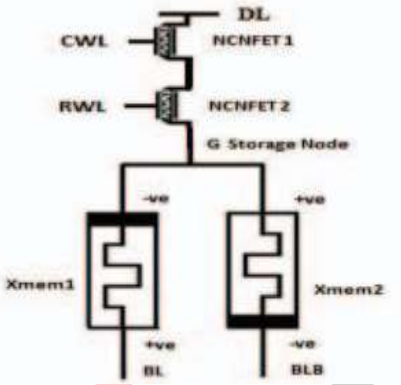

Figure 4. Proposed 2CNFET-2M RRAM circuit.

B. Read Operation

Bit lines BL and BLB both should be discharged to ground before the beginning of read operation. Then row word line RWL and column word line are turned on for a short span of time. One of the bit lines BL or BLB gets charged in a different rate from the other depending on the data stored in Xmem1 and Xmem2. If previously Xmem1 was in high resistive state and Xmem2 was in low resistive state, BL charges up in a faster pace compared to BLB. This is Read-1 operation. In a similar way if Xmem1 was in low resistive state and Xmem2 was in high resistive state BLB gets charged quickly compared to BL and this is called read-0 operation. RWL and CWL are kept on only for a short span so that data in the storage node doesn't get affected.

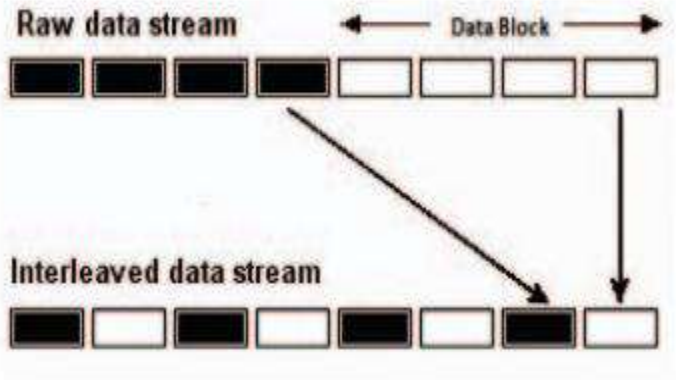

Figure 5. Bit Interleaving scheme

C. Hold mode

During hold mode, both row word line and column word line are pulled down to ground and two bit lines are also pulled down to ground. No operation is carried out in hold mode but still some power is consumed due to connection between and ground which is static power or hold power. Using power reduction technique like MTCMOS technique hold power can be reduced. We have used this technique in our proposed circuit to minimize hold mode power.

IV.SIMULATION RESULT

Linear drift model of memristor by HP Labs and CNFET technology has been used for the simulations. Proposed RRAM cell is compared to previously proposed TG based 2T2M RRAM cell. Tables I and II show the simulated results for write and read access time of the proposed 2CNFET-2M RRAM cell. Write access time for write-1 and write-0 operations and also read access time for read-1 and read-0 operations is displayed.

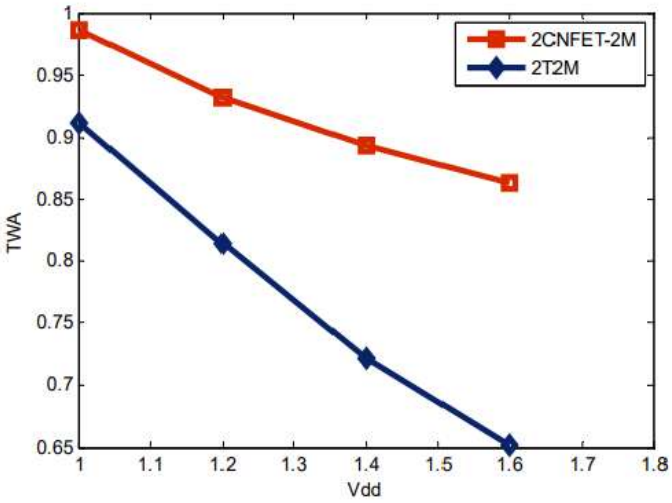

Figure. 6: Comparison of Write Operation for 2CNFET-2M and 2T2M.

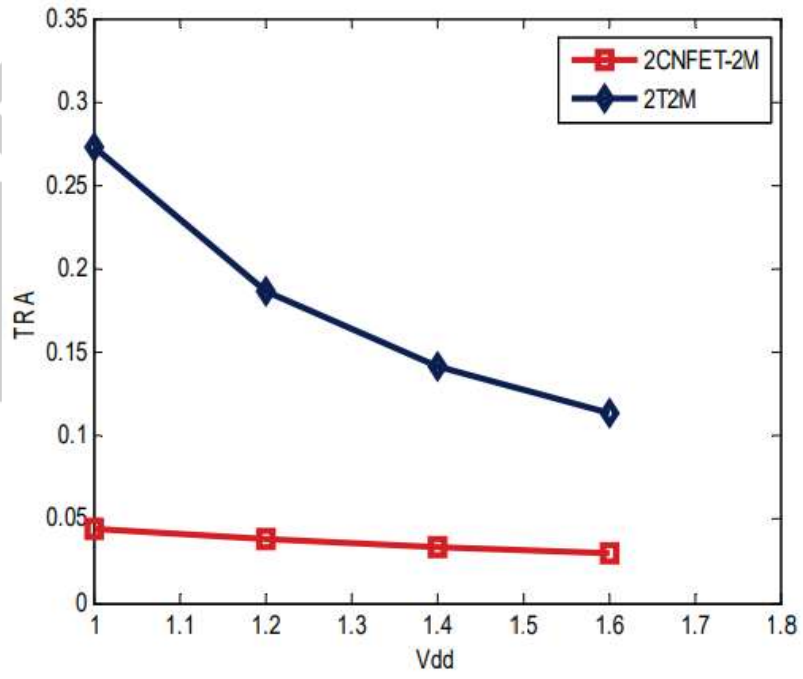

Figure 7: Comparison of TRA for 2CNFET-2M and 2T2M.

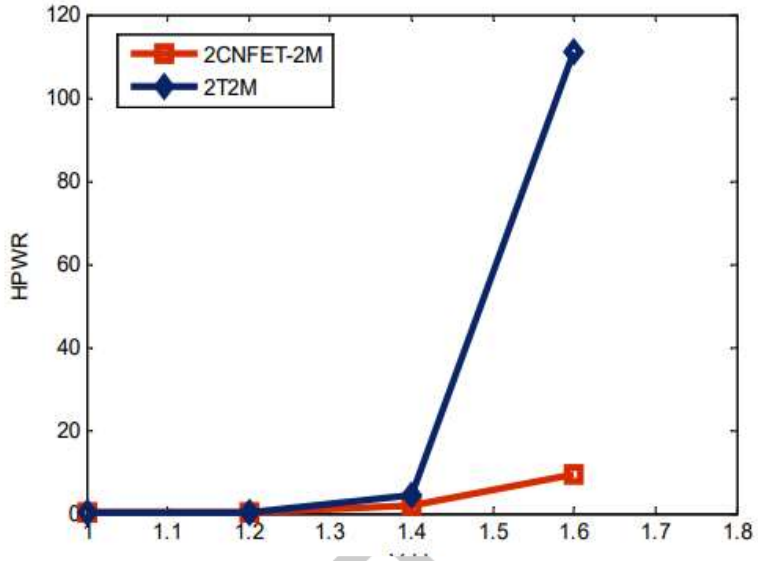

Figure 8:.Comparison of Hold Power for 2CNFET-2M and 2T2M.

V. CONCLUSION

A new CNFET and memristor based low power robust 2CNFET-2M RRAM cell is presented in this paper. The memory cell is non-volatile due to the presence of memristor element. Since read operation is differential, the proposed cell is more immune to PVT variations. Also it is more power efficient compared to conventional SRAM cell and saves area. Moreover, results obtained from simulation show that read and write delays are comparable to conventional SRAM cell and half select tissue is solved. Therefore, proposed RRAM cell is a suitable candidate for future memory applications.

REFERENCES

1. Semiconductor Industry Association (SIA), International Technology Roadmap for Semiconductors 2011 Edition. [Online].
2. V. Sakode, F. Lombardi and J. Han, "Cell design and comparative evaluation of a novel 1T memristor-based memory," 2012 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), Amsterdam, 2012, pp. 152-159.
3. Chua, L.O. Memristor – the missing circuit element. IEEE Trans. Circuit Theory, vol. CT-18, no. 5, p. 507 – 519, Sep. 1971.
4. Chandramauleswar Roy, Aminul Islam, "TG Based 2T2M RRAM Using Memristor as Memory Element," Indian Journal of Science and Technology, vol. 9, no. 33, pp. 1-5, Sep. 2016. DOI: 10.17485/ijst/2016/v9i33/99508.
5. Yanan Sun, Volkan Kursun, "Uniform carbon nanotube diameter and nanoarray pitch for VLSI of 16nm P-channel MOSFETs", VLSI and System-on-Chip (VLSI-SoC) 2011 IEEE/IFIP 19th International Conference on, pp. 226-231, 2011. International Conference on Computer Design, pp.142-147, October 2011.
6. Islam, Aminul & Akram, M Waqas & Pable, Sachin & Hasan, Mohammad. (2010). Design of a Novel CNFET-Based 1-Bit Full Adder in Deep Submicron Technology.
7. Ahmed M. El-Naggar, Mohamed E. Fouda, Ahmed H. Madian, Ahmed G. Radwan, "Reactance-less RM relaxation oscillator using exponential memristor model", Microelectronics (ICM) 2016 28th International Conference on, pp. 361-364, 2016.
8. D. Yu, H. H. C. Iu, Y. Liang, T. Fernando and L. O. Chua, "Dynamic Behavior of Coupled Memristor Circuits," in IEEE Transactions on
Circuits and Systems I: Regular Papers, vol. 62, no. 6, pp. 1607-1616, June 2015.
9. A. P. Chandrakasan and R.W. Brodersen,"Minimizing power consumption in digital CMOS circuits," Proc. IEEE, vol. 83, No. 4, pp. 498–523, Apr. 1995.
10. K. Roy, "Leakage power reduction in low-voltage CMOS designs," Electronics, Circuits and Systems, 1998 IEEE International Conference on, Lisboa, 1998, pp. 167-173 vol.2.
11. Low power and High Speed 13T SRAM Cell with Bit-Interleaving Capability SK Sharma, BP Shrivastava- International Journal of computer Application (IJCA),2016/5.
12. J. Deng, N. Patil, K. Ryu, A. Badmaev, C. Zhou, S. Mitra, and H. S. P. Wong, "Carbon nanotube transistor circuits: Circuit-level performance benchmarking and design options for living with imperfections," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, Feb 2007, pp. 70– 588.
13. Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High performance silicon nanowire field effect transistors," *Nano Letters*, vol. 3, no. 2, pp. 149–152, 2003. [Online]. Available: http://dx.doi.org/10.1021/nl025875l
14. X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai "Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors," *Phys. Rev. Lett.*, vol. 100, p. 206803, May 2008.
15. . C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A graphene field-effect device," *IEEE Electron Device Letters*, vol. 28, no. 4, pp. 282–284, April 2007.
16. T. Ashley, A. R. Barnes, L. Buckle, S. Datta, A. B. Dean, M. T. Emery, M. Fearn, G. Hayes, K. P. Hilton, R. Jefferies, T. Martin, K. J. Nash, T. J. Phillips, W. A. Tang, P. J. Wilding, and R. Chau, "Novel insb-based quantum well transistors for ultra-

high speed, low power logic applications," in *Proceedings. 7th International Conference on Solid-State and Integrated Circuits Technology, 2004.*, vol. 3, Oct 2004, pp. 2253–2256 vol.3.
17. C. I. Kuo, H. T. Hsu, C. Y. Wu, E. Y. Chang, Y. Miyamoto, Y. L. Chen, and D. Biswas, "A 40-nm-gate inas/in0.7ga0.3as composite-channel hemt with 2200 ms/mm and 500-ghz ft," in *2009 IEEE International Conference on Indium Phosphide Related Materials*, May 2009, pp. 128–131.
18. S. L. Hurst, "Multiple-valued logic: its status and its future," *IEEE Transactions on Computers*, vol. C-33, no. 12, pp. 1160–1179, Dec 1984.
19. P. C. Balla and A. Antoniou, "Low Power Dissipation MOS Ternary Logic Family," *IEEE Journal of Solid-State Circuits*, vol. 19, no. 5, pp. 739–749, Oct 1984.
20. A. Heung and H. T. Mouftah, "Depletion/enhancement CMOS for a Lower Power Family of Three-valued Logic Circuits," *IEEE Journal of Solid-State Circuits*, vol. 20, no. 2, pp. 609–616, Apr 1985.
21. D. A. Rich, "A Survey of Multivalued Memories," *IEEE Trans. Comput.*, vol. 35, no. 2, pp. 99–106, Feb. 1986. [Online]. Available: http://dx.doi.org/10.1109/TC. 1986.1676727.
22. Y. Yasuda, Y. Tokuda, S. Zaima, K. Pak, T. Nakamura, and A. Yoshida, "Realization of Quaternary Logic Circuits by n-channel MOS Devices," *IEEE Journal of Solid-State Circuits*, vol. 21, no. 1, pp. 162–168, Feb 1986.