DIAGNOSIS OF ELECTROCARDIOGRAM SIGNAL USING MACH-ZEHNDER INTERFEROMETER TYPE FIR FILTER

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Abstract: In modern days, very large scale integration technologies plays a vital role in consumer products, space and defence applications. Hence, recent scientific researchers focused more on achieving low power, area and delay. Here the FIR Filter is designed for detecting the cardio diseases using optical Reversible and mach-Zehnder Interferometer type. The operations of the Arithmetic Logic Unit are directly depending upon on both adders and multipliers. In normal ALU computation, the traditional Multi-Input Floating Gate based reconfigurable logic, conventional CMOS and normal reversible gate based designs are utilized for these days. Since, there is a problem that occurs in terms of heat, power loss and transmission delay. Therefore, this research focused on providing low power arithmetic computations. The major objective of this research is to provide low power and delay in ALU computation. Next, the utilization of Look up Table is optimized. In this research, the reversible logic gates are considered for constructing arithmetic and logic units as existing module. Then, proposed design depends upon optical reversible logic gates with signed Vedic multiplier for reducing the partial products and its results are better than existing design. So this result in design of the FIR Filter is very simple. In addition, the classification of the diseases is implemented by using Fuzzy classification. The overall module is designed using Verilog Hardware Description Language and tested with the help of Xilinx 14.5. The proposed method has the minimum delay of 24.266ns and the power as 2.78mW. It is noticed that the proposed method has improved by 2.06479% difference. The Proposed FIR filter design is applied for the removal of noise in Electrocardiogram signal and features are extracted using the standard signal properties and classified using fuzzy logic. The proposed method produced the best results as compared to the existing method.

Keywords: Adders; Reversible logic gates; Optical reversible gates; Vedic Multiplier;

I. INTRODUCTION

In the five-generation level of the computing era we are in Fifth generation, so that in the sub field of Integrated circuit is Very Large Scale Integration. The Main parameters of VLSI are Area, Power and Delay. Currently we are using 0.18nm technology for better applications. DRDO designed VIKRAM 1601 Floating Point Processor only for Aeronautical Applications. The Origin of ALU starts from 1968 where Fairchild designed the first Arithmetic Logic Unit in Integrated Circuit. While designing the ALU there are various challenges are faced by the engineer, such as high computational complexity, achieving low power then previous designs and transmission delay. The complexity leads to high cost and data loss occurs due to heat dissipation. For eliminating heat dissipation low power ALU is designed.

Here in major applications, reversible gates are used to reduce the power consumption and loss of data. This type of gates is first introduced in thermodynamic level. Rolf William Landauer first proposed the basic reversible computing technique in 1963. In 1973, Bennet given the theory of computation in biotechnology level, which is the basement of reversible level [1] .Later, Tommaso Toffoli and Edward Fredkin, invented the reversible gates in their name, which was Toffoli Gate, and Fredkin Gate. Pawel Kerntopf studied the remaining gates, which is Peres, Sayem respectively [2]. In 1985,Feynman given the solution that are faced by quantum physics which is based on Toffoli, Fredkin and Bennet[3].In Reversible logic there are many parameters such as number of reversible gates, constant inputs, the number of garbage outputs and quantum Cost.

This is the era of reversible computing, since one of the applications in reversible computing is optical computers. Now-a -days the research is going on in this area. Optical reversible computing is one of the most promising fields for designing high speed and low power consuming future computers. Recently, many researchers have been concentrated on chip level implementation of the optical circuits. Thus realizing an efficient adder is required for better performance of an ALU and therefore the processor. Another important element in an ALU after adder is a multiplier.

The technology of reversible computing is frequently developed. In further, reversible computing on all the circuits is designed. Lala et al., (2010) designed the adder circuits in reversible logic. For decreasing factors of area and power [4] are compared. Pan and Nalasani (2005) presented the logical reversibility [5]. The inputs and outputs of this type of gates can be uniquely retrievable from each other. The information is secured and cannot erase. The operation performed in this type of circuit is backward so that it is only less power. Vedral et al., (1996) represented an addition and modulo computations in research level [6]. In the field of biotechnology itself the reversible gates are designed. The major applications of reversible logic is low power CMOS and optical information processing, DNA computing, quantum computation and nanotechnology. It is the n x n logic device, which is ‘n’ inputs and ‘n’ outputs.

The major contribution of this research is to design an advanced Arithmetic Logic Unit with less complexity. It is mainly design with the help of Signed Vedic Multipliers and Carry Select adders. The internal blocks of such adders and multipliers are framed with optical reversible gates constructed by the Mach-Zehnder Interferometer (MZI) under the Semiconductor Optical Amplifiers (SOAs) strategy.

In signal processing, a finite impulse response (FIR) filter is a filter whose impulse response (or response to any finite length input) is of finite span, since it settles to zero in finite time. This is as opposed to infinite impulse response (IIR) filters, which may have inner input and may keep on reacting indefinitely (generally rotting). The impulse response (that is, the yield in response to a Kronecker delta contribution) of a Nth-order discrete-time FIR filter keeps going precisely N + 1 tests (from first nonzero component through last nonzero component) before it at that point settles to zero. FIR filters can be discrete-time or continuous-time, and digital or analog.

Further, this paper is organized as follows. Section 2 reviews some critical events in arithmetic and logical events and its demerits. Next, the existing module with reversible logic gates are designed and simulated, and it verifying the delay and power consumption factors. Then, the proposed methodology is framed with the help of optical reversible logic gates and the Vedic multiplier units under section 3. The simulated results are discussed under section 4. Finally, the research is summarized in the section 5.

II. LITERATURE REVIEW

Sun and Jiang (2010) identifies the problems that are occurred in conventional structures namely, complex structure, adder independent structure and tree structure and chain structure. David et al., (2005) described the complex structure with the combination of arithmetic and logic operations in a single unit. In such cases, various control signals are used to control each activities, decides the complexity. Similarly, the Prakash and Saxena (2009) considered the adder independent structure separately for arithmetic operations and an individual module performs logic operations, it provides huge complexity. Zhou and Guo (2008) presented the tree structure that organizes a set of functional components as a tree. Here, the operation performs like a chain for each component/operation.

The conventional ALU designs are framed with different styles namely, transistor level (Ryu et al., 1999),Feedback Switch Logic based ALU (Prakash and Saxena 2009), ALU using Novel 8T full adder and Pass transistor logic based multiplexers (Nehru et al., 2012), Clock gating based energy efficient ALU design (Pandey et al., 2013) etc. Up to now, various researchers focussed on implementing the ALU design. While combining various operations some internal fault may occur. To identify and detect the fault, Veeravalli (2009) implemented the error-detection mechanisms for regulating the faults arrived during computation. The internal Boolean unit suggested finding the alternate solution to the hardware units. Whenever, an error occurs during the active ALU processing, replacement is carried out with the sparse ALU. Various fault tolerance mechanisms are executed for managing the redundancy and avoid unwanted mechanism.

Syamala and Tilak (2011) demonstrated the ALU concept with the help of reversible logic gates by using multiplexers and control signals. In this type of ALU applications, they had designed only four basic arithmetic logical operations on two n-bit operands. Some suggestion is carried out in terms of the production of garbage outputs and constant inputs. Most of the logics utilizes the frequently used for random logic for error detecting and correction. Yelekar and Chiwande (2011) also considered the reversible gate to a build more complicated circuits such as sequential and combinational circuits. It designed the adder concept using reversible peres gate and TSG gate. Mamun and Menville (2014) framed a 'Selim Al Mamun' (SAM) gate with the performance metrics like quantum cost, delay and garbage outputs. Mainly, the SAM gate is designed to manage the performance of memory elements in recent developments.

Some reversible latches are presented over all computation for improving the sequential circuits. In any type of circuit, there is a need for low power consumption. Since, the sequential elements consume more power than combinational. The process of combining the memory elements decides the overall performance. Singh and Goel (2015) framed an adder and subtractor using reversible logic gates. Since, lot of innovative reversible concepts are publishing since, there is a limitation like combinational delay, transition delay, computation time and power utilization. Nielsen and Chuang (2000) described about the quantum error correction in all arithmetic operations. Thapliyal and Ranganathan (2010) represented a conservative logic in terms of various combinational structures.

Biswas et al., (2014) concentrated on quantum computing with the help of various designs. Coarse-grained architecture, on the other hand, is typically much larger, and may consist of ALUs and possibly even a significant amount of storage. There is a need for developing the reconfigurable architecture with various processes. For processing such cases, the low power architectures are considered with various multipliers and adder logics. The Vedic multipliers are considered for effective speed of computation. The reversible circuits are considered for reducing the power dissipation with the information/bits loss as in but in the case irreversible circuit limited to some errors. Power gating technique is incorporated in the architecture to reduce the power consumed by the overall ALU. Recently, Swamynathan and Banumathi presented a 32-bit ALU using Verilog HDL with the logical functions. The design was implemented in Xilinx. The design of an ALU and a Cache recollection for use in a high performance processor was

examined. Reversible logic vital in recent years because it has competency to reduce the power dissipation which is main requisite in low power design. ALU which are designed for utilizing non reversible logic gates consume more latency.

A review of various ALU design approaches in computing system for various architectures are considered to find the merits and de-merits of various designs. Most of the researchers discussed above have the same objective of minimizing the power consumption of the adder, multiplier and memories. In adder designs some control input technique are degraded and creates complexity. To avoid such complexity, various reversible logic gates are considered with more transistors and possess high power dissipation. The limitations of conventional adders are fan out and high computation cost. Similarly, multipliers also consume more power because of high switching activity. To avoid all such limitations, the enriched ALU is to be designed.

Patel et al., (2014) has Been Enlivened By The Need To Locate An Effective Technique For ECG Flag Analysis Which Is Basic And Has Great Precision And Less Calculation Time. For Investigation The ECG Signals From MIT Database are Utilized. The Underlying Errand For Productive Examination Is The Expulsion Of Clamor And Detection Of QRS Tops. It Really Includes The Extraction Of The QRS Part By Dismissing The Foundation Clamor. This Assignment Is Finished Utilizing Pen Tompkins Algorithm. The Second Undertaking Include Figuring Of Heart Rate, Detection Of Tachycardia, Bradycardia, Asystole And Second Degree Av Obstruct From Recognized QRS Crests Utilizing MATLAB. The Outcomes Demonstrate That From Recognized QRS Tops, Arrhythmias, Which Depend On Increment Or Abatement In The Quantity Of QRS Top, Nonappearance Of QRS Pinnacle Can Be Analyzed.

Jagatap, et al., (2012) R proposed the method of ECG Signal for the investigation of heart diseases. ECG feature extraction plays an important job in the cardiac diseases. One cardiac cycle in an ECG signal consist of the P-QRS-T waves. It has amplitude and interval esteem which determines the functioning of heart of each human. ECG estimates the rate and regularity of heartbeat. It displays the electrical activity of the heart in type of wave line on the paper. The ECG Signal is conducted with the data compression and reconstruction. Today such a large number of research and techniques have been developed for breaking down the ECG signal. The information will then investigated and characterized on premise of compression method, fuzzy logic, etc.

Ojha et., al., (2014) has performed the study and examine the Electrocardiograph (ECG) waveform to detect abnormalities, with presence with reference to P, Q, R and S peaks. The first phase incorporates the acquisition of constant ECG data. By the next phase of generations, the signal is pursued by pre-processing stage. Thirdly, the procured ECG signal is subjected to feature extraction. The extracted features detect unusual peaks present in the waveform thus the typical and unusual ECG signal could be differentiated in light of the features extracted. The work is implemented in the most well-known multipurpose tool, MATLAB. This software efficiently employments algorithms and techniques for detection of any abnormalities present in the ECG signal. Proper utilization of MATLAB functions (both built-in and client characterized) can lead us to work with ECG signals for processing and examination continuously applications. The simulation would help in improving the precision and the equipment could be built conveniently.

III. RESEARCH METHODOLOGY

The following section provides the detail description of traditional methodology and its description. In recent days, the Mach-Zehnder interferometer (MZI) based optical switch has attracted many researchers in the field of all optical reversible logic. Hence, this optical gate was constructed with three inputs and three outputs reversible gate with mapping of inputs (A, B, C) to output as shown in the equation 3.1. Figure 1 indicates the Mach-Zehnder Interferometer Logic Gate.

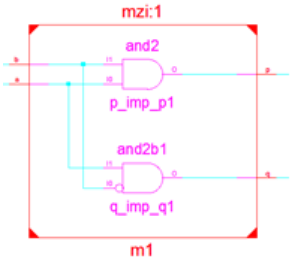

Fig 1: Mach-Zehnder Interferometer Logic Gate

$$P = AB + (A \oplus B)\, C \tag{3.1}$$

$$Q = A \oplus B,\ R = A\,(\text{invB}) + (A \oplus B)\, C \tag{3.2}$$

From the equation 3.1 and 3.2, the fan out are represented by P and Q. The working of the MZI can be clarified as:

(i) When there is an approaching input sign at port A and the control motion at port B, at that point there is a light present at the yield bar port B. Here, there is no light present at the yield cross port,

(ii) Without control motion at input port B and approaching sign at input port A then the fan out of MZI are exchanged and brings about the presence of light at the yield cross port and no light at the bar port.

The optical implementation of an optical reversible gate, which is shown in figure 2. It contains 3 MZI based Switches, 4 Beam Splitters (BS) and 3 Beam Combiners (BC). From the figure 2, the BC denotes the combination of optical beams while the beam

splitter simply. Taraphdar et al., (2010) coined out the optical reversible circuits for all basic gates. Likewise, this research is followed for designing the arithmetic and logical gates.

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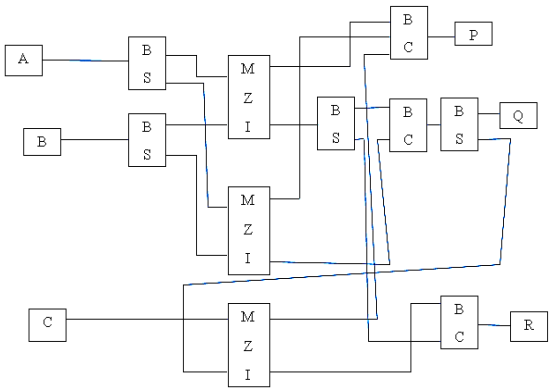

Fig 2 Optical Reversible Gate I

3.1 Different Types of Reversible Gates

The arithmetic and logic unit designs are framed with the help of reversible logic gates to perform high speed, low power with minimum computation complexity. It is framed with the help of reversible gates namely, Feynman gate, Fredkin Gate and Peres gate. Initially, the combinations of proposed reversible logics are carried out here as an overview. Finally, the combinations of all reversible gates are constructed and designed with low power ALU module.

3.1.1 Feynman gate

In this gate A, B are the inputs and P, Q are the outputs. This Feynman gate is motivated from the Kotiyal et al., (2012). It is totally an optical illustration of the Feynman gate. The Feynman gate (FG) is a 2 inputs and 2 output reversible gate. It is represented in the equation 3.3.

$$P=A \text{ and } Q=A\oplus B \qquad (3.3)$$

Where A, B are the inputs and P, Q are the outputs, respectively.

This gate is also termed as Controlled-Not gate (CNOT) when the input A=1 then its output Q has the complement of B. It is normally implemented with 2 MZI optical switches, 2 beam combiner (BC) and 2 beam splitter (BS) in all optical reversible computing. The designed Feynman gate is shown in the figure 3.

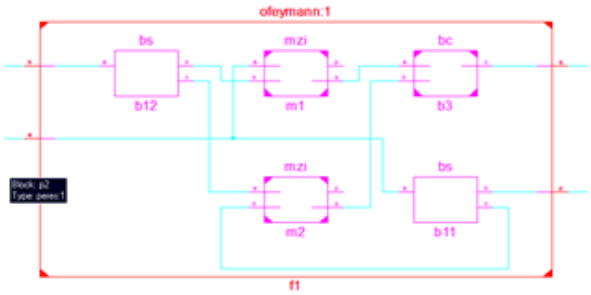

Fig 3: Feynman gate

3.1.2 Fredkin Gate

Fredkin gate (FRG) is called as controlled permutation gate. Normally, Fredkin gate is a universal gate for designing complex circuits to minimize the fan out. Here, the FRG is design and implemented by other reversible components like BS, BC and MZI units. As shown in the figure 4, the output of Fredkin Gate is the operation of multiplexer in with the first input as a status line. Its input vector has the hamming weight that is equal to hamming weight of its output vector. Reversible 3*3 gate maps inputs contains the variable A, B and C. the output representation is listed in equation 3.4 to 3.6.

$$P=A \qquad (3.4)$$

$$Q=A'B+AC \qquad (3.5)$$

$$R=AB+A'C \qquad (3.6)$$

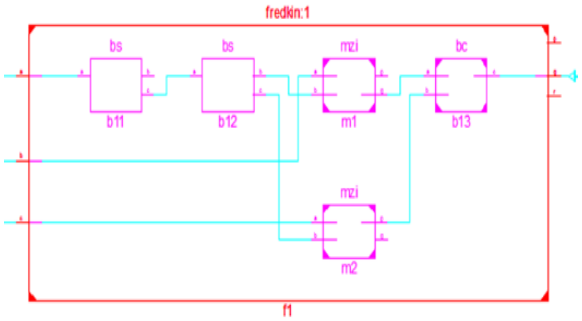

Fig 4: Fredkin Gate

3.1.3 Peres Gate

The output of Peres gate is a combination of both Feynman and Toffoli Gate. The combination of both logics simplifies the design and provides proper output similar to normal conventional Peres gate. It is designed with normal X-OR gate and Feynman gate for minimizing the quantum cost. For better performance in speed and power, we are designing reversible gates using semiconductor Optical amplifiers. With help of these amplifiers, Mach-Zehnder Interferometer (MZI) is designed. The Peres gate is represented with respect to the equations 3.7 to 3.9.

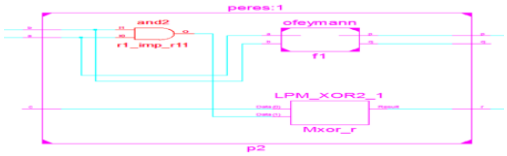

Fig 5: Peres Gate

$$P = A \quad (3.7)$$
$$Q = A \oplus B \quad (3.8)$$
$$R = AB \oplus C \quad (3.9)$$

3.2 FIR FILTER USING ALU COMPONENTS

In this, the traditional FIR filter is designed using optical reversible concept and MZI. This filter is applied to the ECG signal to remove the noise. The removal of noise is an important for the classification of signal based on the diseases.

The filtered FIR ECG signal undergoes the process of feature extraction using entropy, skewness, and kurtosis. The extracted features are used for the classification of diseases using fuzzy logic.

Fuzzy classification is the way toward grouping elements into a fuzzy set whose enrolment function is characterized by the truth-value of a fuzzy propositional function.

$$\sim C = \{i \mid \sim \Pi\ (i)\}$$

A fuzzy class is characterized as a fuzzy set ~C of people I fulfilling a fuzzy classification predicate ~π which is a fuzzy propositional function. The area of the fuzzy class operator ~{ .| .} is the set of factors V and the set of fuzzy propositional functions ~PF, and the range is the fuzzy power set (the set of fuzzy subsets) of this universe, ~P(U):~{ .| .}:V × ~PF ⟶ ~P (U)

A fuzzy propositional function is, closely resembling, an articulation containing at least one factors, with the end goal that, when values are doled out to these factors, the articulation turns into a fuzzy suggestion in the feeling of.

Steps for performing the FIR on ECG signal:

Pre-processing:

- The ECG signal is converted into binary format and stored in a text file using MATLAB.
- This text file is called in XILINX to perform the noise removal process using proposed FIR Filter design.

Noise Removal:

- This operation is performed to prove two factors one is that the proposed FIR filter able to remove the noise efficiently when compared to the traditional design and second factor is the proposed FIR design consumes less power and LUTs as compared to the reversible FIR filter
- Then the filtered ECG signal is converted into a text file for further processing.

Feature Extraction:

- The filtered signal's text file is converted into a signal by using MATLAB.
- Then the signal undergoes feature extraction by calculating chip histogram features like kurtosis, skewness, Entropy.
- Then, the membership functions for fuzzy classification is formed based on the features extracted from the signal.
- Then, the signals are classified using fuzzy and estimated by accuracy, sensitivity and specificity.

As shown in the figure 7, the proposed ALU is designed. It is specifically designed with the reversible gates. The description of each arithmetic block is explained below. Apart from that logical blocks such as AND, OR, NAND, NOR, XOR and XNOR are

similar to the past logics. The modifications are carried out in adder, multiplier and subtractor. Since, literature review stated that there is a complexity in multiplier design. Hence, we concentrated more on internal units of multiplier. Further, some stages of adders are also constructed with the help of modified peres gate and feynmen gate logics. Table 1 indicates the overall computation process with 15 stages of selection lines.

Table 1: Truth table for proposed logic

S3	S2	S1	S0	OPERATION	DESCRIPTION
0	0	0	0	RESULT=A+B	HALF ADDER
0	0	0	1	RESULT=A+B+CIN	FULL ADDER
0	0	1	0	RESULT=A-B	SUBTRACTOR
0	0	1	1	RESULT=A*B	MULTIPLIER
0	1	0	0	RESULT=A+1	INCREMENTER
0	1	0	1	RESULT= A-1	DECREMENTER
0	1	1	0	RESULT=A&B	AND LOGIC
0	1	1	1	RESULT=A|B	OR LOGIC
1	0	0	0	RESULT= Inv A	COMPLEMENT
1	0	0	1	RESULT=~(A&B)	NAND LOGIC
1	0	1	0	RESULT=~(A|B)	NOR LOGIC
1	0	1	1	RESULT=A^B	XOR LOGIC
1	1	0	0	RESULT=~(A^B)	XNOR LOGIC
1	1	0	1	RESULT=SHIFT A	BARREL SHIFT
1	1	1	0	COMPARE (A,B)	COMPARATOR

Since the ALU is selected according to the selection inputs S_3 S_2 S_1 and S_0. The final output of the ALU is determined by the set of multiplexers and with the input selection lines. The function table for the ALU is completely determined by the input selection. Based on the combination of the output pins are selected.

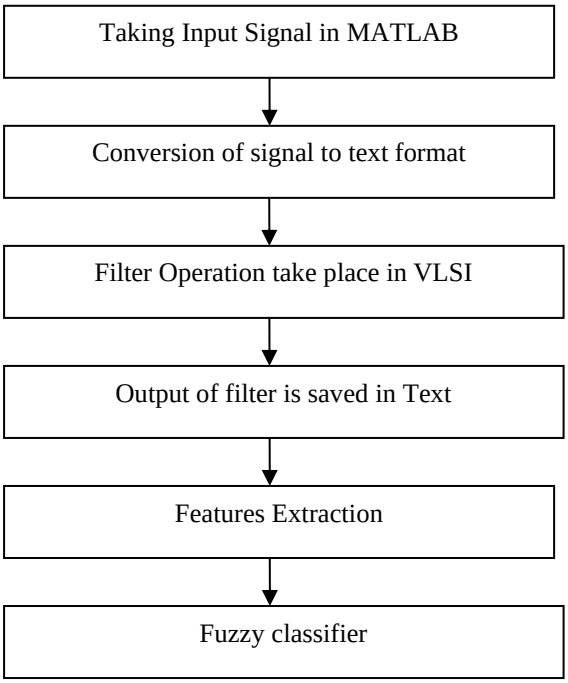

Fig 6:Block Diagram of the Sysetm

3.2.1 Adder

The adder is one of the basic element in the arthimetic computation. It decides the complexity of the whole system. The process of providing the low power is a key motive, but still the reduction of adder units are difficult. Hence, with the new idea of reversible logic a new adder is designed with binary to excess converter and multiplier. Figure 8 shows the tradtional adder design and its internal block optical full adder is shown in the figure 9. Similarly, the internal block of optical full adder is designed with basic 2 beam combiner (BC) and 4 beam splitter (BS) with 2 MZI component, which is shown in the figure 10. This operation intiates the half adder operation through the selection bits S_3, S_2, S_1, S_0 as 0000 and for full adder the S_3, S_2, S_1, S_0 will be 0001.

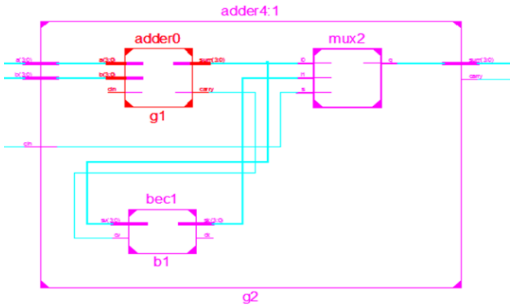

Fig 7: Adder design with binary to excess converter and multiplexer

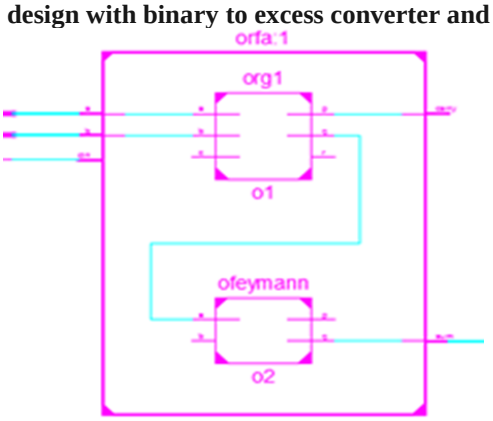

Fig 8: Adder design with optical full adder

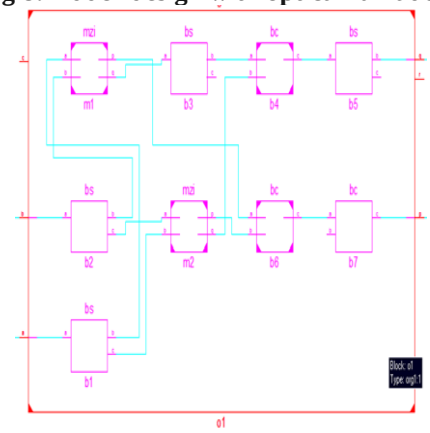

Fig 9: Optical full adder design

3.2.2 Subtractor

For subtraction, some conventional methods uses addition of 2's complement of subtrahend to the minuend. In such case of operation, the complexity increases to great extent. Hence, a reversible a comparator with countable X-OR logic gates are used to limit the complexity. The comparator helps to minimize the computational complexity and increases the way of obtaining the low power. Figure 11 provides the RTLview of comparator and figure 12 proves that the subtractor framed with the comparator. This operation intiates the operation through the selection bits S_3, S_2, S_1, S_0 as 0010.

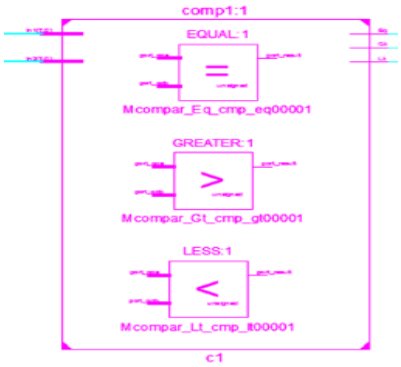

Fig 10: RTL view of Comparator

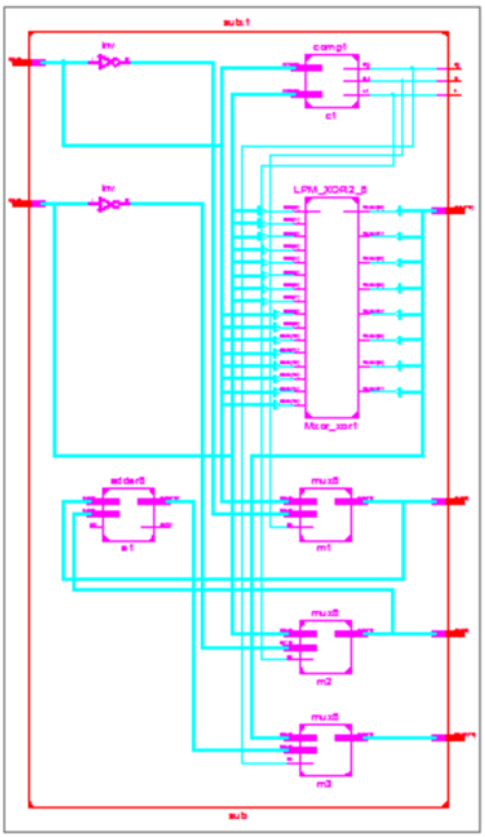

Fig 11: RTL view of Subtractor

The main advantage of this subtractor is to process simultaneously and displays the artimetic outcome exactly. The composition of various internal units decides the carry and borrow of previous stage. The combination of multiplexer provides the numerous support to XOR logic and provide exact result.

3.2.3 Multiplier

Low-power multipliers are very important for reducing energy consumption of digital processing systems. This research provides the experience of applying an reversible version of our logic gates and adders on multipliers for high-speed and low-power purposes. Here, the computational steps are reduced to filter out the useless power. It is framed with the signed vedic multiplier and combination of adder for partial product generation unit with the help of multiplexer. Here the figure 13 displays the flow of signed vedic multiplier. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. It is the design of high speed Vedic Multiplier using the techniques of Ancient Indian Vedic Mathematics that have been modified to get better performance.

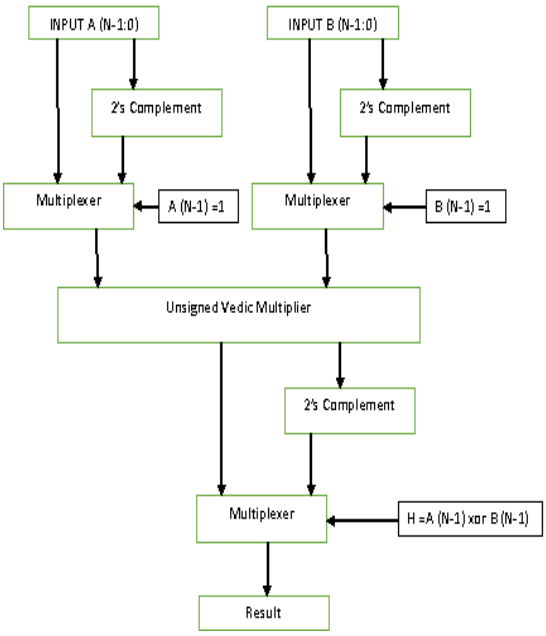

Fig 12: Signed Vedic Multiplier

The RTL schematic view of 2x2 bit Vedic multiplier is similar to that of 2x2 bit conventional Array Multiplier. It is implemented by four input AND gates and two half-adders. The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules. Similarly, 8X8 bit Vedic multiplier is implemented using four 4x4 bit Vedic multiplier. Here, the input bit streams are considered with the various (N-1) terms. Based on the Most Significant Bit (MSB), the multiplexer decides the operation of unsigned or signed. Hence, for example if N=8, then the operation turns towards the unsigned multiplication and skips the 2's complement stage if A_7 bit is logic high and vice versa. The unsigned vedic multiplier contains carry select adder and 2*2 vedic multiplier.

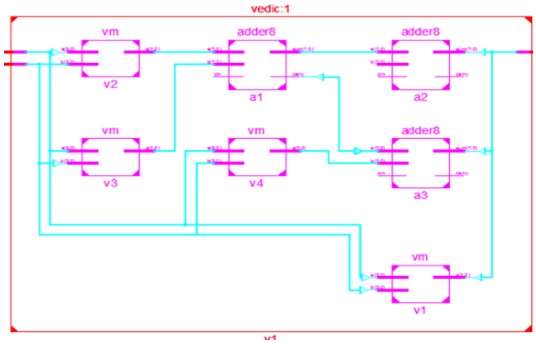

Fig 13: Unsigned Vedic multiplier

In Carry select adder, two adders are used while one adder is for carry '0' position and other is for carry '1' position. Here carry input is the signal selected from the multiplexer and processed with the AOI logic, which is represented in the figure 15. AND-OR-Invert (AOI) logic are two-level compound logic functions constructed from the combination of one or more AND gates followed by a NOR gate. It is simpler and more efficient than the sum of the individual gates. The major outcome of this AOI implementation is to raise speed, reduce power, and potentially ensure lower fabrication cost.

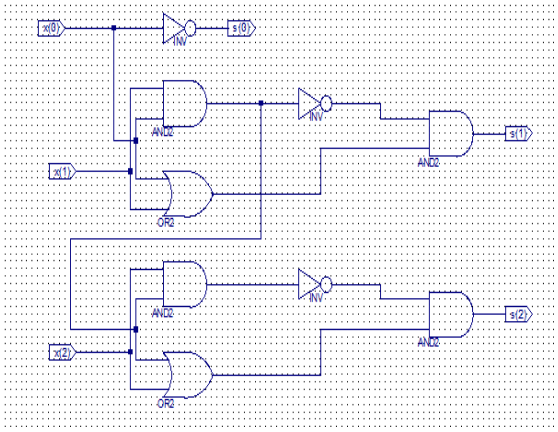

Fig 14: Logical diagram of AOI Converter

The following steps are considered for signed Vedic multiplication.

Step1: Initially, the inputs and outputs are declared.

Step2: Analyse the MSB bit of both inputs and decides the signed and unsigned operation.

Step 3: Now the negative numbers are in 2's complement form should convert to normal representation. Then, subtract the number with 4 bits of combination in the case of 2x2Vedicmultipliers and 16 bit combination.

Step 4: After converting the numbers execute the reversible unsigned Vedic multiplier.

Step 5: Output will be signed multiplication that provides the exact computation.

IV. EXPERIMENTAL RESULTS

Table 2: Comparison Results

Parameters	**8 bit Existing reversible system**	**8 bit Proposed optical reversible system**	**FIR filter design using reversible system**	**FIR filter optical reversible system**
LUTs	426	413	347	279
Power (mW)	2.838	2.78	38.16	37.69

The overall design modules are tested with the help of Xilinx 14.5 integrated synthesis environment. The internal logical blocks are designed with the Verilog module to minimize the coding complexity. The internal blocks are minimized so that the flow of the computation will be exactly reduced.

Table 2 denotes the experimental results of existing ALU with normal CMOS operation and which is compared with the proposed reversible logics based ALU unit. The total power consumption of the proposed module is termed as 2.78mW. It is dynamically varied due to the internal computation process. Since, the carry flag is avoided to minimize the delay and avoid over computation. The output verification is determined as shown in the figure 16. Similarly, the utilization of look up table is reduced to great extent.

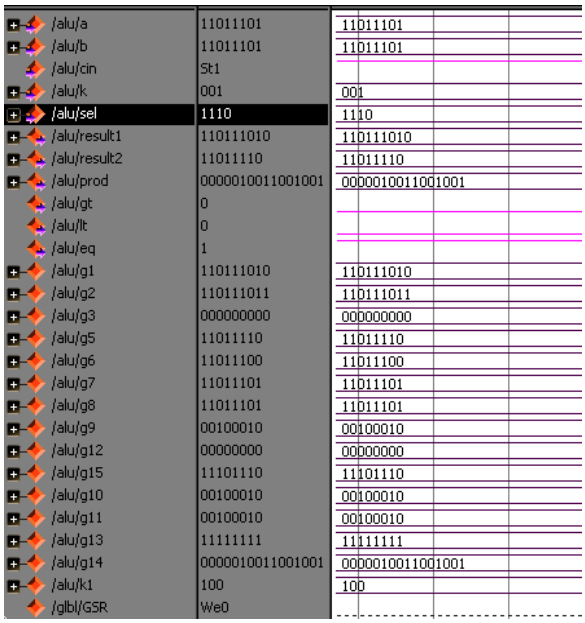

Fig 15: Simulated result for ALU design

The noise removal and classification of ECG signal is performed with the help of MATLAB and Xilinx. The MATLAB is used for the conversion of signal to binary and vice versa. The feature extraction and classification using MATLAB. The Xilinx is used to perform the noise removal process using optical reversible and MZI FIR filter.

The analysis is performed on the four types of the ECG signal as follows:

Normal Sinus Rhythm

The ECG signal will be of the normal Waveform and the heartbeat will fall between 60 and 100.

Bigeminy

It is otherwise known as premature ventricular contraction in which the heartbeats are not normal and the ECG signal will have alternating signal of long and short heartbeats.

Ventricular arrhythmia

It indicates the heart attack to the patients by the abnormalities of ECG signal which is from the ventricles. It also indicates the damage of the heart muscle.

Ventricular tachycardia

It shows the faster heart rate of the patient which is obtained from the ventricles of the heart.

The below figures are the analysis of the four types of ECG signals.

Normal Sinus Rhythm

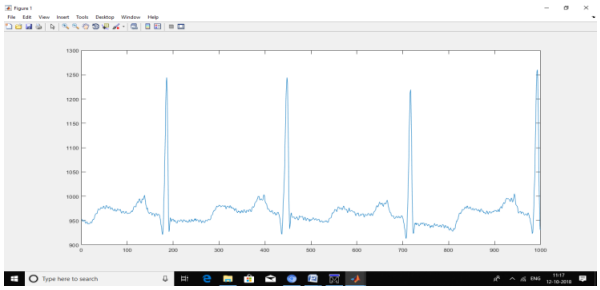

Fig 16: Input Signal

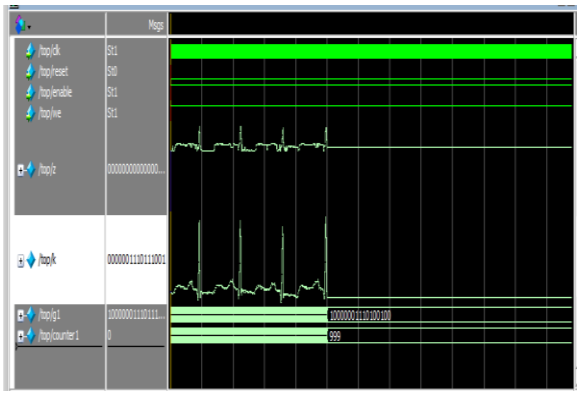

Fig 17: Modelsim Output of the Filtered Signal

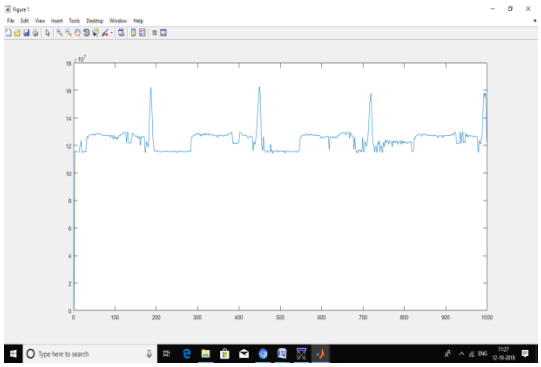

Fig 18: MATLAB Output of the Filtered Signal

Bigeminy

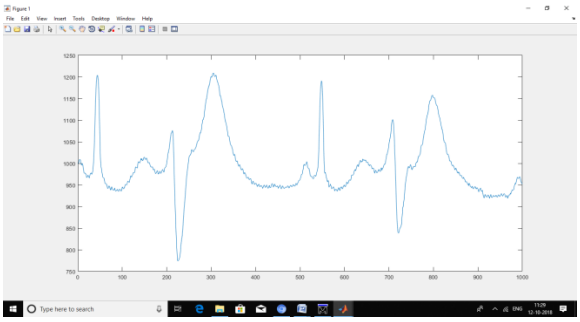

Fig 19: Input Signal

Fig 20: Modelsim Output of the Filtered Signal

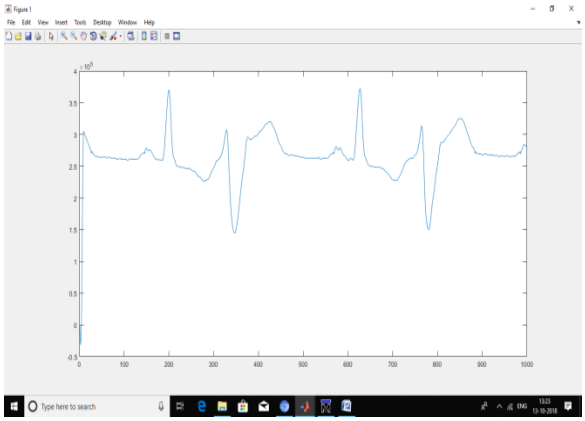

Fig 21: MATLAB Output of the Filtered Signal

Ventricular arrhythmia

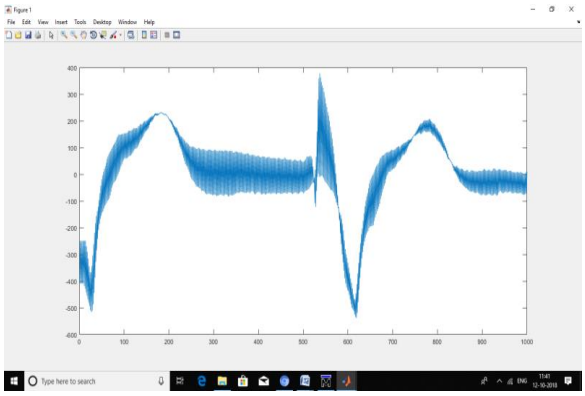

Fig 22: Input Signal

Fig 23: Modelsim Output of the Filtered Signal

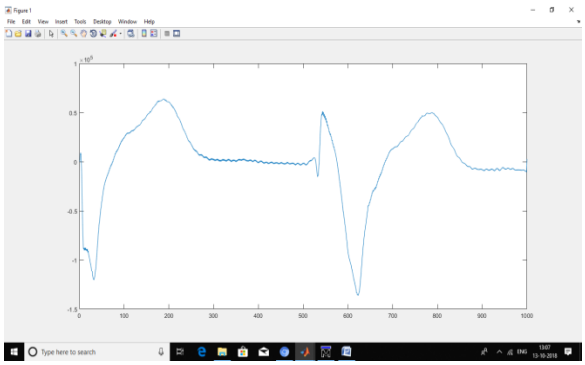

Fig 24: Matlab Output of the Filtered Signal

Ventricular tachycardia

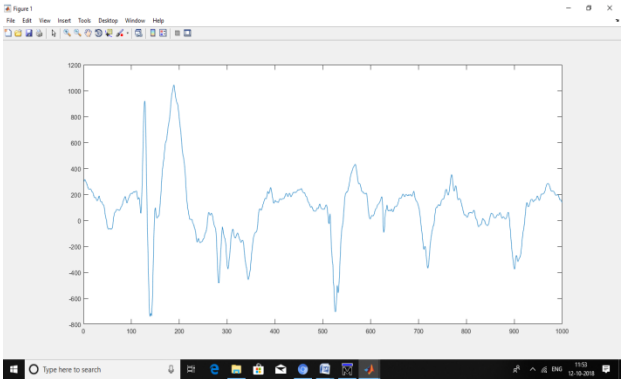

Fig 25: Input Signal

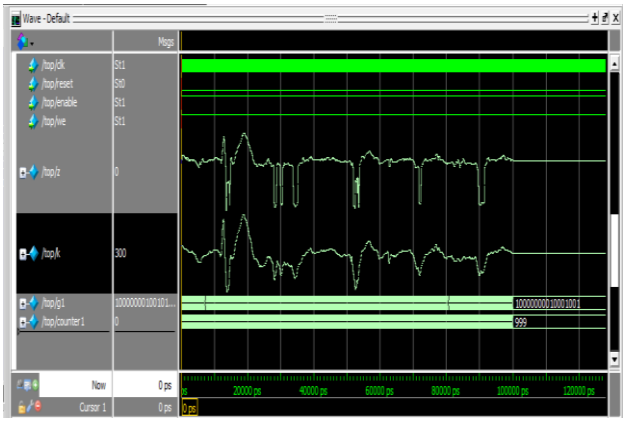

Fig 26: Modelsim Output of the Filtered Signal

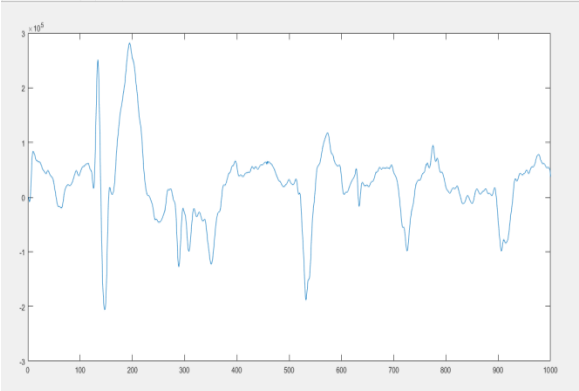

Fig 27: Matlab Output of the Filtered Signal

Table 2: Comparison Results for classification

Method	Accuracy (%)	Sensitivity (%)	Specificity (%)
Reversible FIR filter	81	62	66.8
Optical Reversible FIR filter	95	81.4	71.4

From the experimental results, it is noticed that the low power objective is achieved. The proposed method also able to classify the Filtered ECG signals better. The process is completely simple and in unique style.

V. CONCLUSION

This research focused on implementing the reversible logical gates with the addition of low power Mach-Zehnder Interferometer (MZI) technique. The design adopts the low power reversible gates in adder designs to simplify the internal

computation. Similarly, the multiplier is designed by equipping the Vedic multiplier and reversible multiplexer to manage the partial products through carry save adder. In addition, the carry save adder is designed with the AOI Converter module for limiting the power overload. Similarly, the traditional methods has designed and synthesized to verify the functionality of proposed reversible MZI based arithmetic and logical unit. The Vedic multiplier implementation with Carry save adder has an extremely high flexibility on adjusting the data computation time. This facilitates the robustness of ALU that can attain 2% power reduction in proposed ALU design when compared with the conventional designs. This design completely verified by using Xilinx14.5 using verilog coding. In this the FIR filter is designed using ALU components and it is used for removal of noise in the ECG signal is verified by its lesser power consumption and better noise removal as compared to the Reversible gate based FIR filter. The proposed FIR filter is suitable for the signal processing applications with less power consumption.

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