EFFICIENT DESIGN OF SHIFT REGISTER FOR AREA AND POWER REDUCTION USING PULSED LATCH

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Abstract— **A shift register is a basic building block in VLSI circuits. Shift registers are commonly used in many applications, such as digital filters, communication receivers and image processing. The architecture of a shift registers is quite simple. An N-bit shift register is composed of a series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption. Because there is no circuit between flip-flop in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches are replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop and it cannot be used in a shift register due to the timing problem between pulsed latches. To overcome this problem, multiple non overlap delayed pulsed clock signals are used instead of the conventional single pulsed clock signal. The shift registers use a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256_bit shift register using pulsed latches have been fabricated using a 0.18μm CMOS process with V_{DD}=1.8V.The core of the area is 1483μm^2. The power consumption is 1.2mW at a 100MHz clock frequency. The above work was carried out using Microwind software. The multiple non overlap delayed pulsed clock signals saves 66% area and 80% power compared to the conventional shift register with flip-flops.**

Keywords—Area-efficient, flip-flop, pulsed clock, pulsed latch

I.INTRODUCTION

In digital circuits, a shift register is a cascade of flip flops. Its sharing the same clock, in which the output of each flip-flop is connected to the data input of the next flip-flop. As resulting in a circuit that shifts by one position the bit array stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input. A shift register may be multidimensional, such that its data in and stage outputs are themselves bit arrays this is implemented simply by running several shift registers of the same bit-length in parallel. These are often configured as serial-in parallel-out (SIPO) or parallel-in serial-out (PISO).. There are also bidirectional shift registers which allow shifting in both directions. The serial input and last output of a shift register can also be connected to create a circular shift register. In digital design flip-flops and latches are basic storage element. Flip flops are timing elements in digital circuits. which have a great impact on speed and power consumption. In VLSI chip design reducing power has become an important consideration of a performance and area. The Shift register is a type of sequential circuit it is mainly used for storage or transfer digital data.

An M-bit shift register consists of M -data flip-flops which are connected in series form. The implementation of the M-data flip-flop is less important element to regulate the capability of the total synchronous circuit than the area and power consumption as a result there is no circuit present between flip-flops within the register. To reduce the area and power consumption, the smaller flip-flop is used for the register. In this flip flops the transistor are more compared to pulsed latches so that the circuit has more switching and power consumption are high. Flip-flops are replaced by pulsed latches in several applications, because pulsed latches are smaller than flip flops. The use of multiple non overlap delay pulsed clock signals by the single pulsed clock signals by this design solves the timing problem in pulsed latches [4]. The shift register uses a less number of the pulsed clock signals and combine the latches to many sub shift registers and exploitation further temporary storage latches.

The data string is presented at Data in, and it is shifted right one stage each time Data Advance is brought high. At each advance, the bit on the far left is shifted into the first flip-flop's output. The bit on the far right is shifted out and lost. The data are stored after each flip-flop on the 'Q' output, so there are four storage. Hence it is a 4-bit Register. To give an idea of the shifting pattern, imagine that the register holds 0000. As Data in10110000 presents to the register. The left hand column corresponds to the left-most flip-flop's output pin. So the serial output of the entire register is 10110000. It can be seen that if data were to be continued to input, it would get exactly what was put in, but offset by four Data Advance cycle. This arrangement is the hardware equivalent of a queue. Also at any time, the whole register can be set to zero by bringing the reset (R) pins high. This arrangement performs destructive readout - each datum is lost once it has been shifted out of the right-most bit.

II. ARCHITECTURE

A. *Previous work for Shift Register*

A master slave flip flop using two latches can be replaced by a pulsed latch. It consists of a latch and a pulsed clock signal [6].All pulsed latches share the pulse generation circuit for the pulsed clock signal.

The area and power consumption of the pulsed latch is small. The pulsed latch cannot be used in shift register due to timing problem, output signal of the first latch (out1) changes correctly because the input signal of the first latch (in1) is constant during the clock pulse width. But the second latch has an uncertain output signal (out2) because its input signal (out1) changes during the clock pulse width.
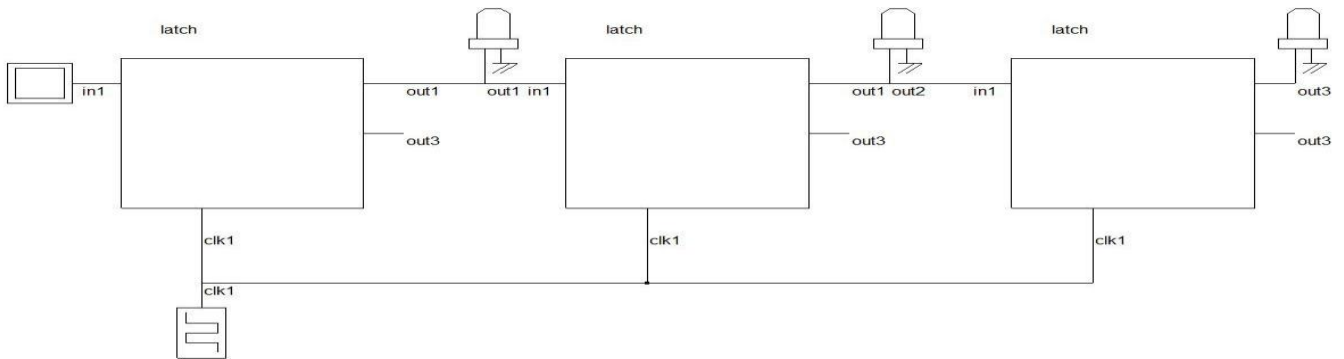
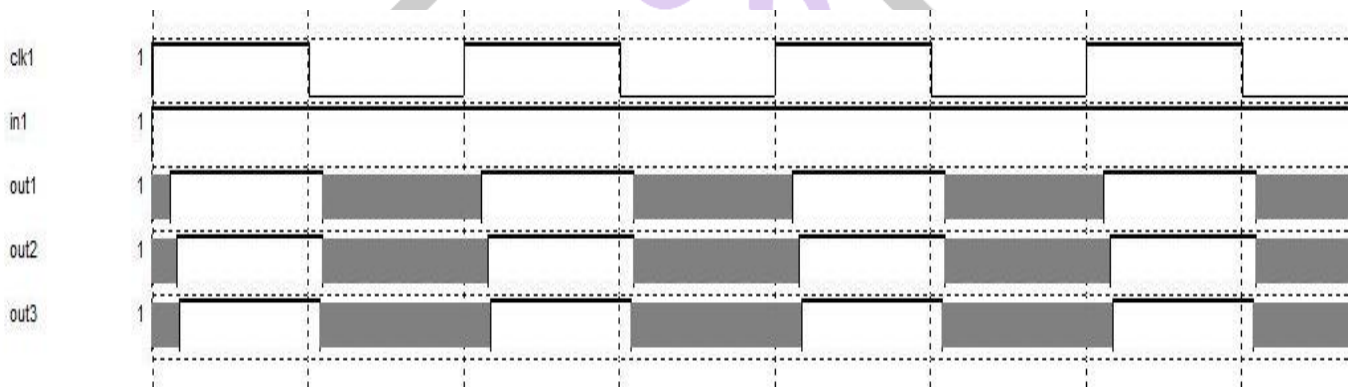Fig.1 Schematic of Shift Register with latches and a pulsed clock signal

Fig.1a Timing Diagram of Shift Register with latches and a pulsed clock signal

One solution for the timing problem is to add delay circuits between latches as shown in Fig.2. The occurrence of the clock pulse is delayed version of the previous latch as shown in Fig.2a.The output signals of the first and second latches (out1 and out2) changes during the clock pulse, but the input signals of the second and third latches become the same as the output signals of the first and second latches after the clock pulse. All latches have constant input signals during the clock pulse and no timing problem occurs between the latches. As a result, the delay circuits cause large area and power overheads.
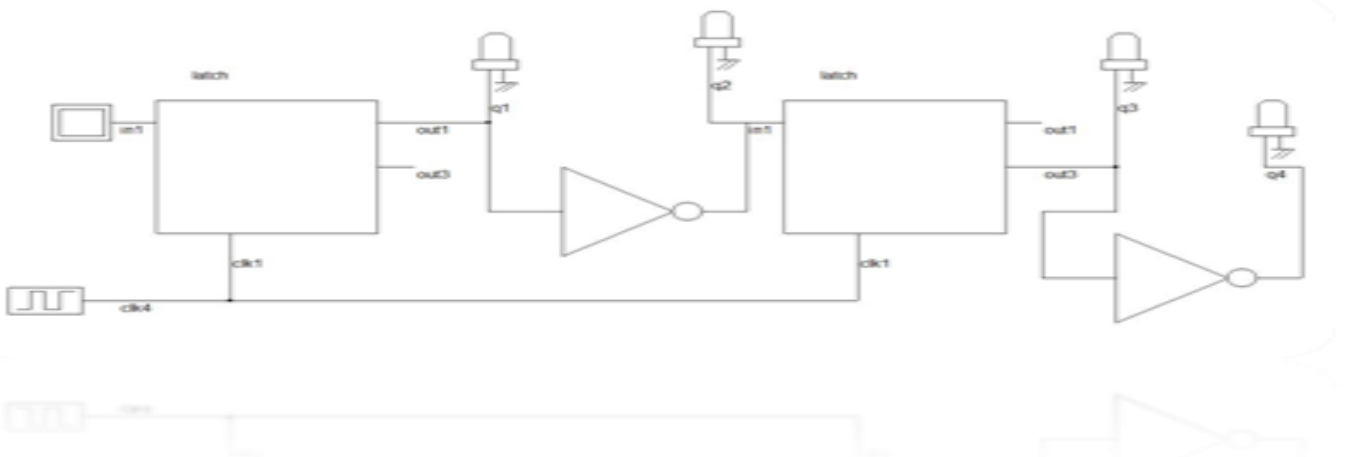
Fig.2 Schematic of Shift Register with latches, delay circuits and a pulsed clock signal
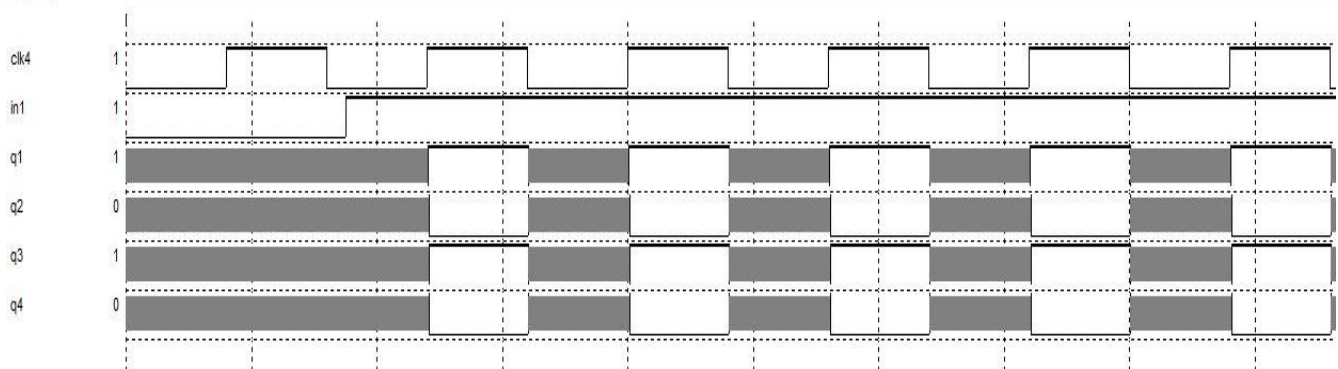
Fig.2a Timing Diagram of Shift Register with latches, delay circuits and a pulsed clock signal

Another solution is to overcome the timing problem is to use multiple non overlap delayed pulsed clock signals, are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. This solution also requires many delay circuits.
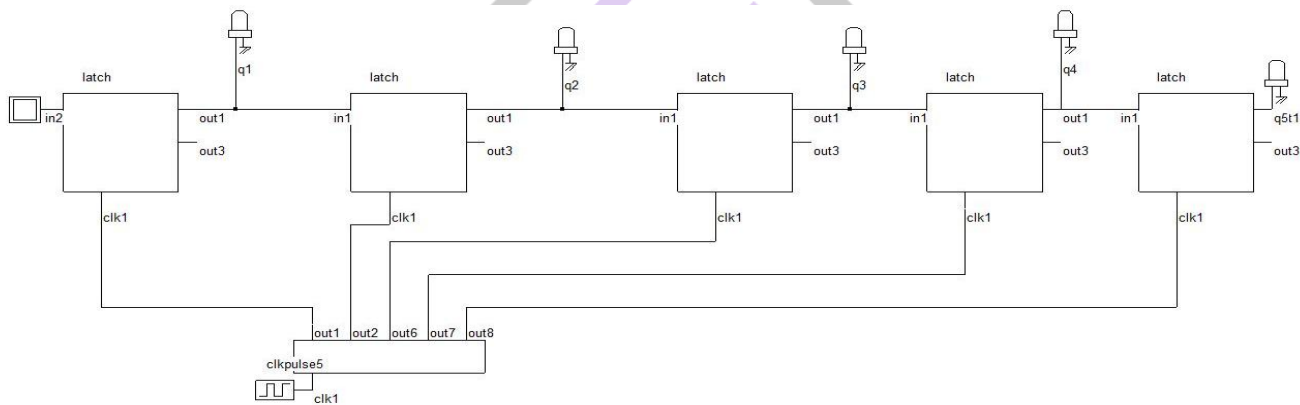

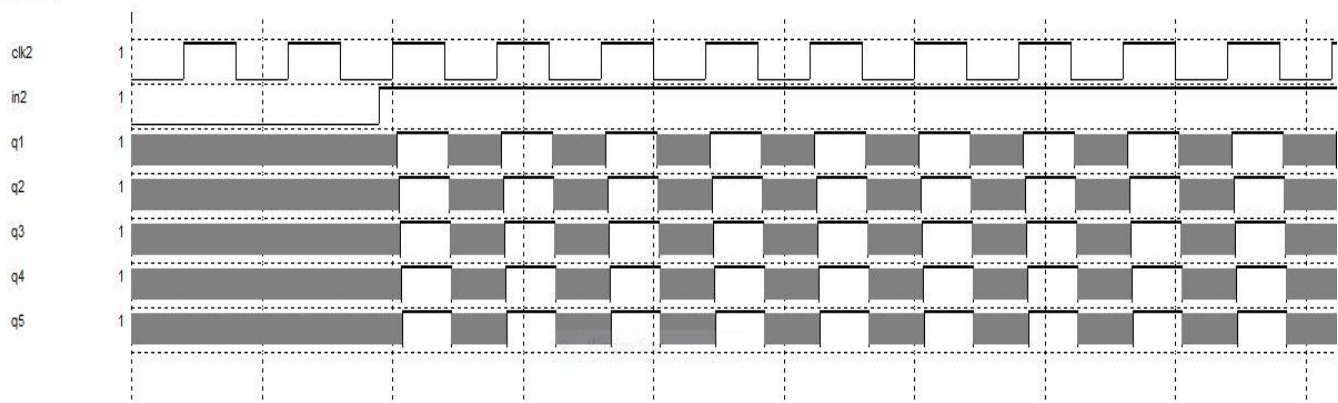Fig.3 Schematic of Shift Register with latches and delayed pulsed clock signals

Fig.3a Timing Diagram of Shift Register with latches and delayed pulsed clock signals

The Shift Register is divided into M sub shift registers in order to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non overlapped delayed pulsed clock signals. In the 4-bit sub shift register #1, four latches store 4-bit data (q1-q4) and the last latch stores 1-bit temporary data (T1), which will be stored in the first latch (q5) of the 4-bit sub shift register #2. The area and power consumption of the 256-bit shift

register according to M, if N=256 and M=4 sub module, each single latch consists of 1-bit. So, total number of latches is 320 and 64 sub module.
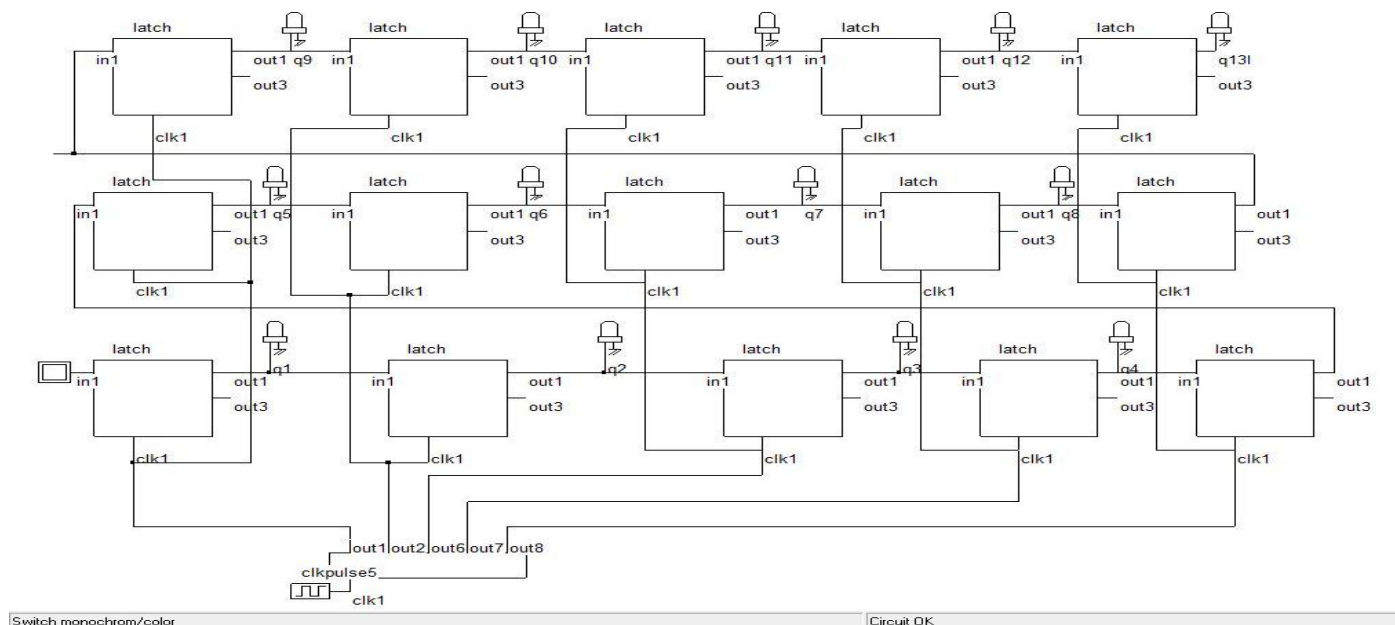

Fig.4 Schematic of Sub shifter Register for 4-bit module

The Shift Register is divided into M sub shift registers in order to reduce the number of delayed pulsed clock signals. A 8-bit sub shifter register consists of nine latches and it performs shift operations with nine non overlapped delayed pulsed clock signals. In the 8-bit sub shift register #1, eight latches store 8-bit data (q1-q8) and the last latch stores 1-bit temporary data (T1), which will be stored in the first latch (q9) of the 8-bit sub shift register #2. The area and power consumption of the 256-bit shift register according to M, if N=256 and M=8 sub module, each single latch consists of 1-bit. So, total number of latches is 288 and 32 sub module. So, compare to 4-bit sub module (M=4), area and power gets reduced.
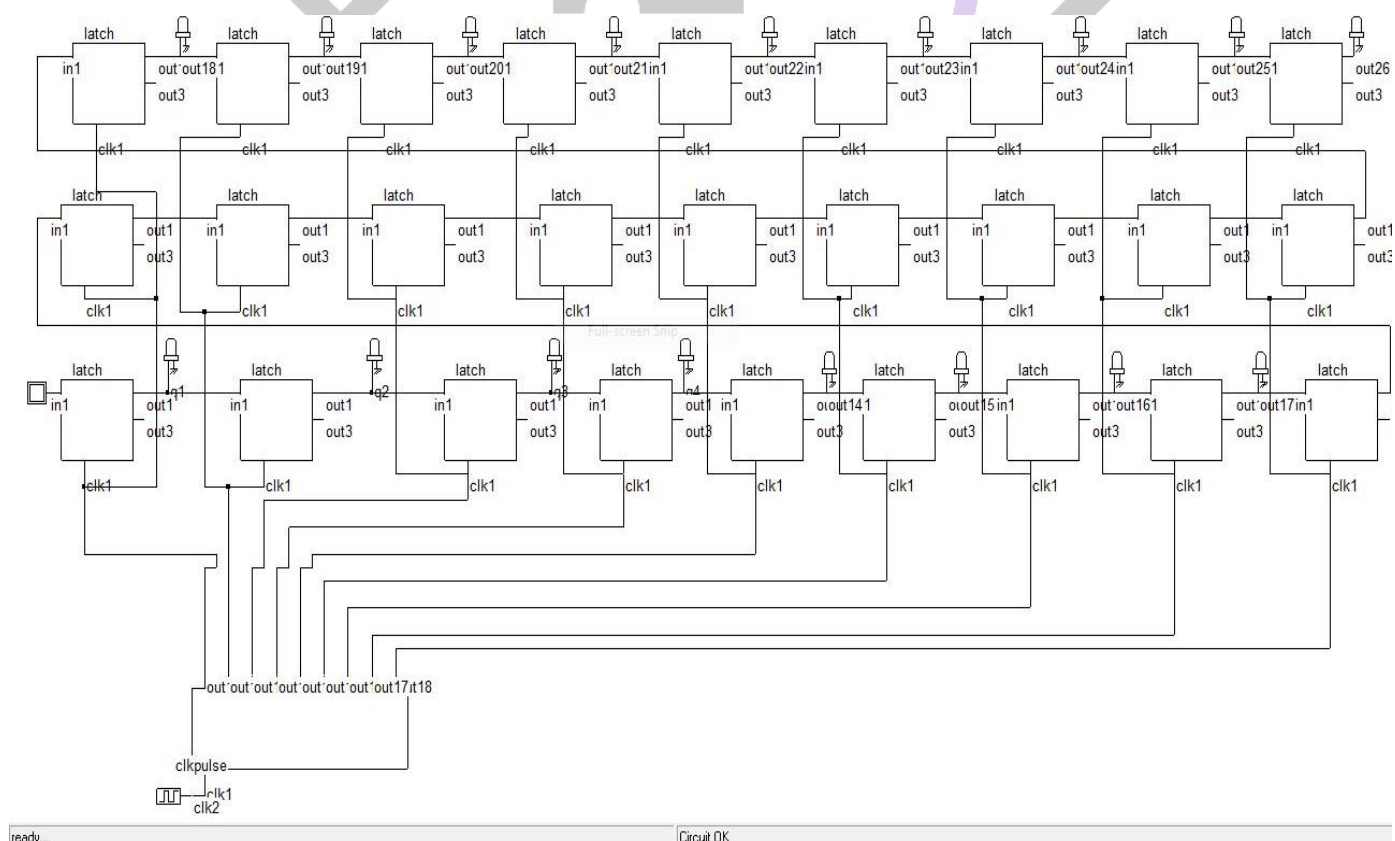

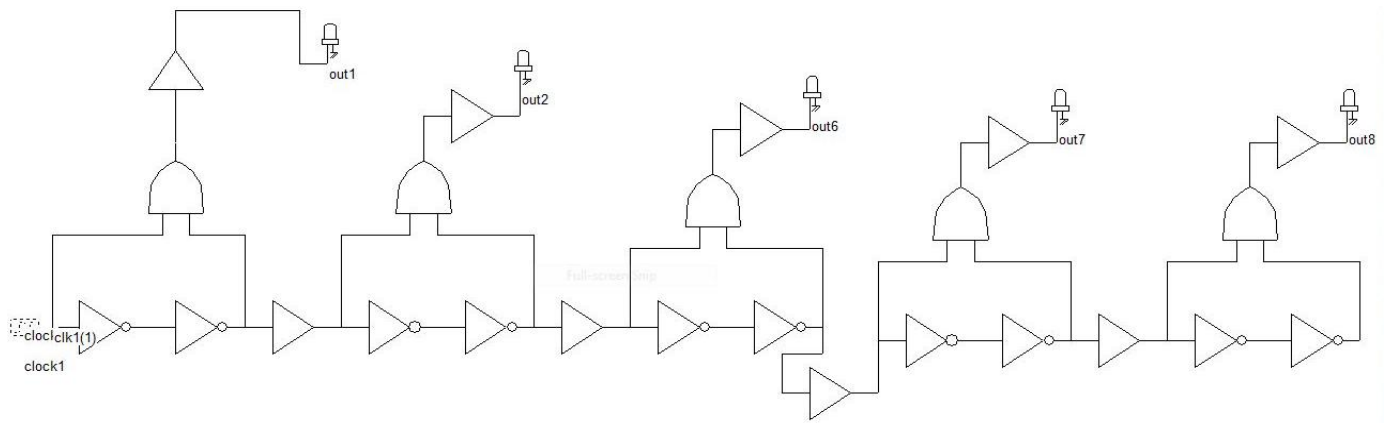Fig.5 Schematic of sub shifter Register for 8-bit module

Fig.6 Schematic of Delayed pulsed clock generator

The numbers of latches and clock pulse circuits change according to the word length of the sub shift register (M). M is selected by considering the area, power consumption, speed.

The area optimization can be performed as follows, when the circuit areas are normalized with a latch, the area of a latch and a clock pulse circuit are 1 and α_A, respectively. The total area becomes $\alpha_A \times (M+1) + N(1+1/M)$.

The power optimization is similar to the area optimization. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and a clock pulse circuit are 1 and α_P, respectively. The total power consumption is also $\alpha_{p\,x}(M+1) + N(1+1/M)$.

B.Proposed work for Shift Register

The Shift Register is divided into M sub shift registers in order to reduce the number of delayed pulsed clock signals. A 4-bit sub shift register consists of five latches. One latch consists of 4-bit.It performs shift operations with five non overlapped delayed pulsed clock signals. In the 4-bit sub shift register #1, four latches store 16-bit data (q1-q4) and the temporary latch stores 4-bit data (T1) from the previous latch which will be input to the first latch (q5) of the 4-bit sub shift register #2. The area and power consumption of the 256-bit shift register according to M, if N=256 and M=8 sub module, each single latch consists of 4-bit. So, total number of latches is 80 and 16 sub module.
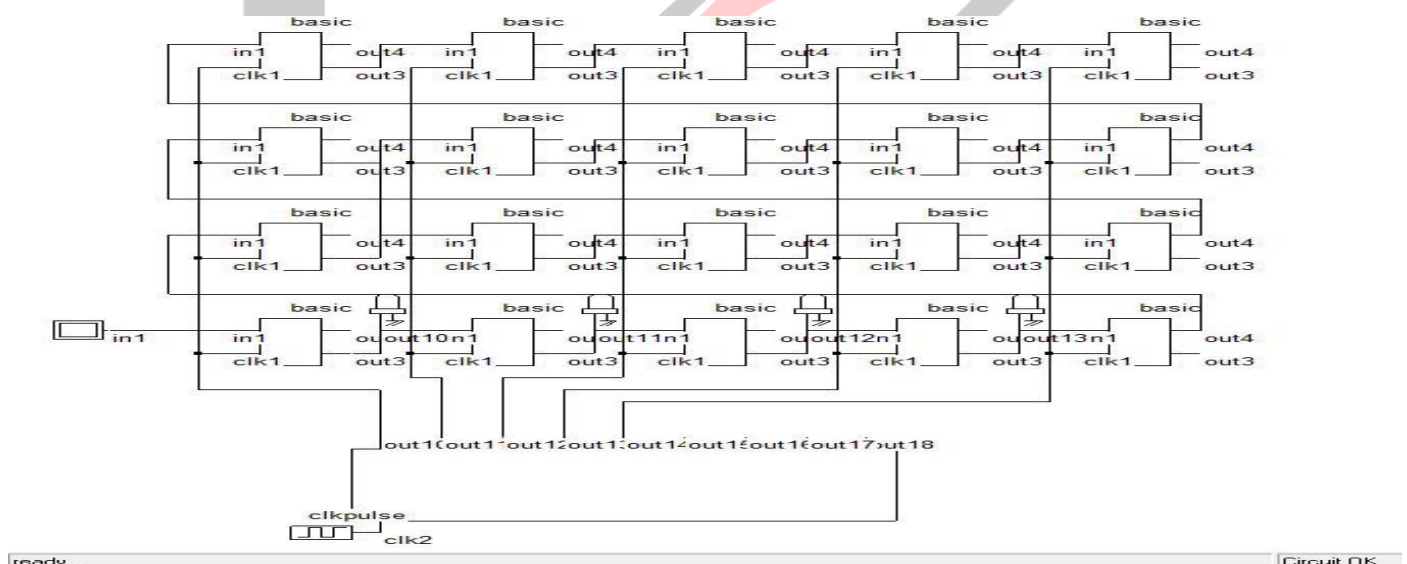

Fig.7 Schematic of sub shifter Register for proposed 4-bit sub module

The Shift Register is divided into M sub shifter registers to reduce the number of delayed pulsed clock signals. A 8-bit sub shifter register consists of nine latches. One latch consists of 8-bit.It performs shift operations with nine non overlap delayed pulsed clock signals. In the 8-bit sub shift register #1, eight latches store 64-bit data (q1-q8) and the last latch stores 8-bit temporary data (T1) which will be stored in the first latch (q9) of the 8-bit sub shift register #2. The area and power consumption

of the 256-bit shift register according to M, if N=256 and M=8 sub module, each single latch consists of 8-bit. So, total number of latches is 36 and 4 sub module. So, compare to 4-bit sub module (M=4), area and power gets reduced.
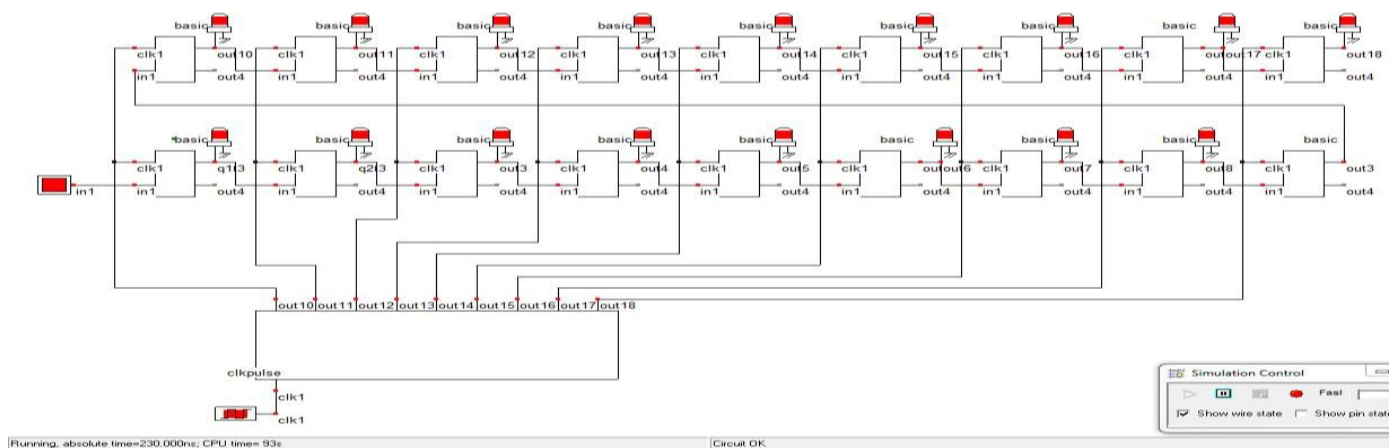

Fig.8 Schematic of sub shifter Register for proposed 8-bit sub module

III. CHIP IMPLEMENTATION

In chip implementation, the Static differential Sense amp Shared Pulse Latch (SSASPL) in Fig.9, Which is the smallest latch. The original SSASPL with 9 transistors [6] is modified to the SSASPL with 7 transistors in Fig.9 by removing an inverter to generate the complementary data input (db) from the data input (d).In the proposal shift register, the differential data inputs (d and db) of the latch come from the differential data outputs (q and qb) of the previous latch. The SSASPL use the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal.
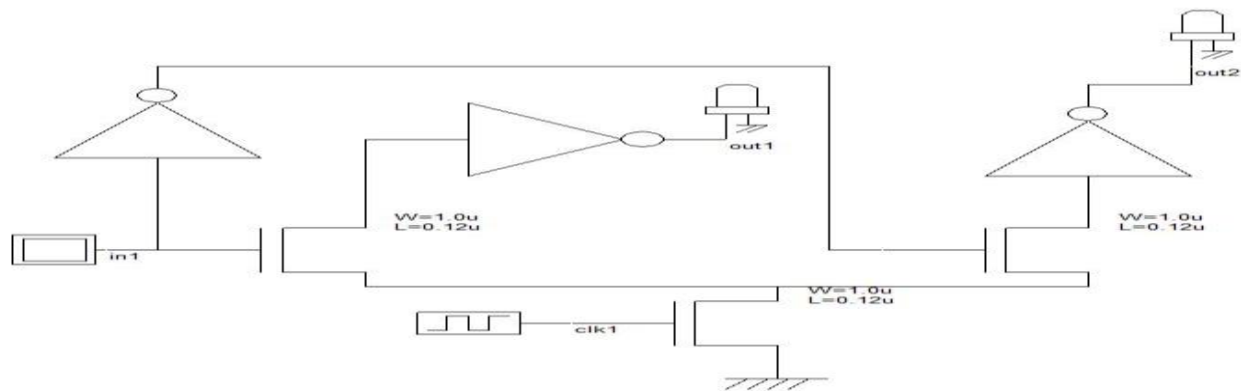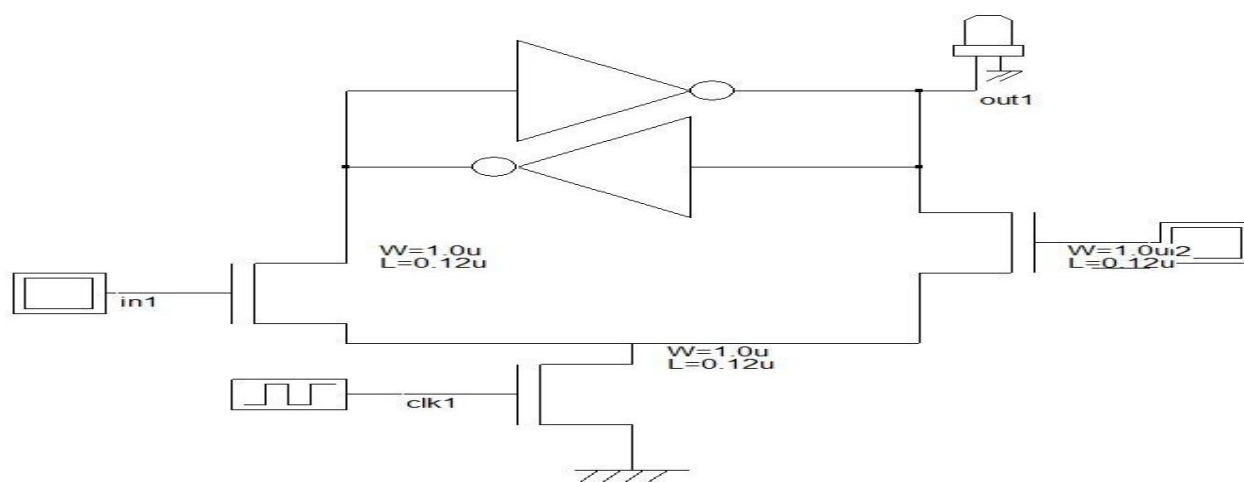

Fig.9 Schematic of original SSASPL

Fig.10 Schematic of modified SSASPL

IV. **PERFORMANCE COMPARISON**

A. **PULSED LATCH:**

TABLE I. PULSED LATCH

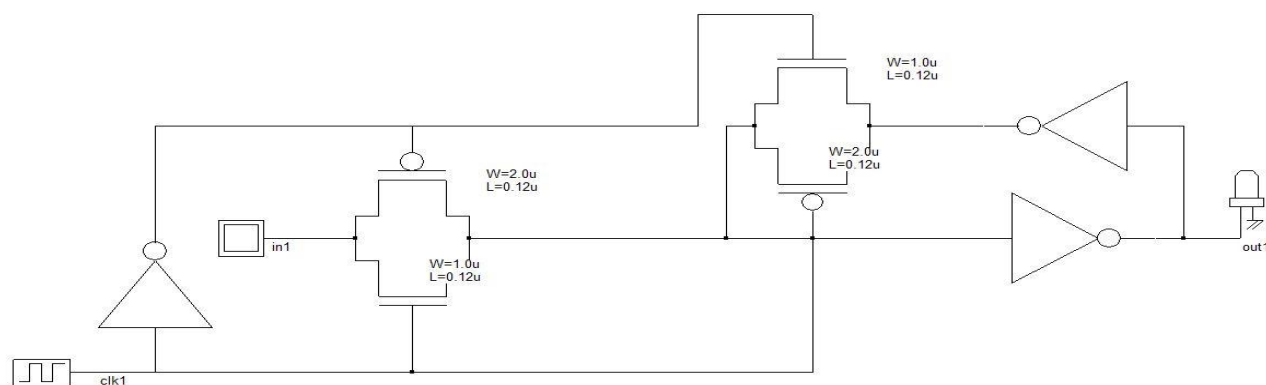|	TYPES	TOTAL NUMBER OF TRANSISTORS	NUMBER OF TRANSISTORS CONNECTED TO CLOCK
PULSED LATCH	STATIC DIFFERENTIAL SENSE AMP SHARED PULSED LATCH	7	1
	TRANSMISSION GATE PULSED LATCH	10	4
	HYBRID LATCH FLIPFLOP	14	2

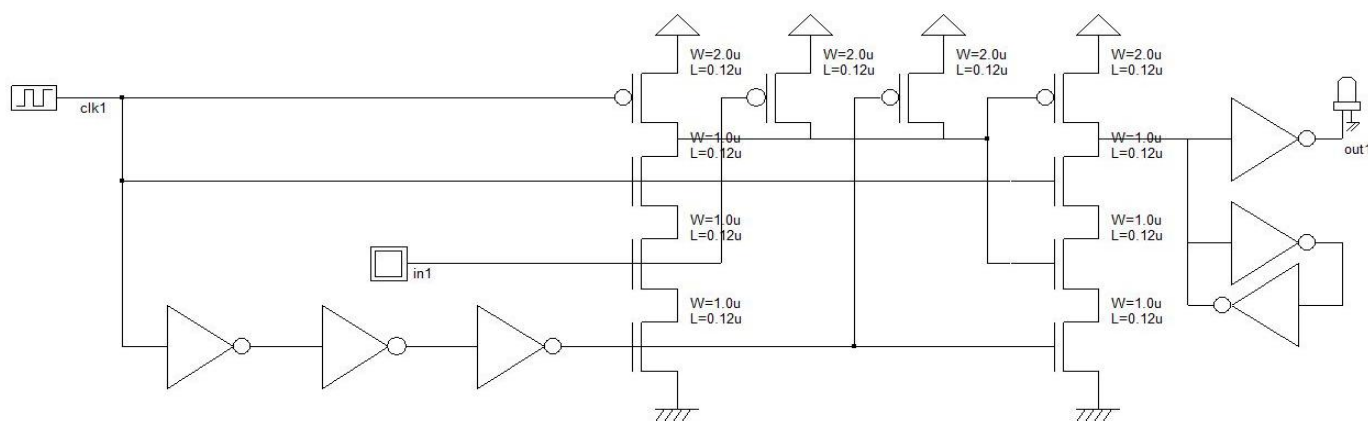Fig.11 Schematic of Transmission Gate Pulsed Latch

Fig.11 Schematic of Hybrid Latch Flip Flop

B. FLIPFLOP:

TABLE II. FLIPFLOP

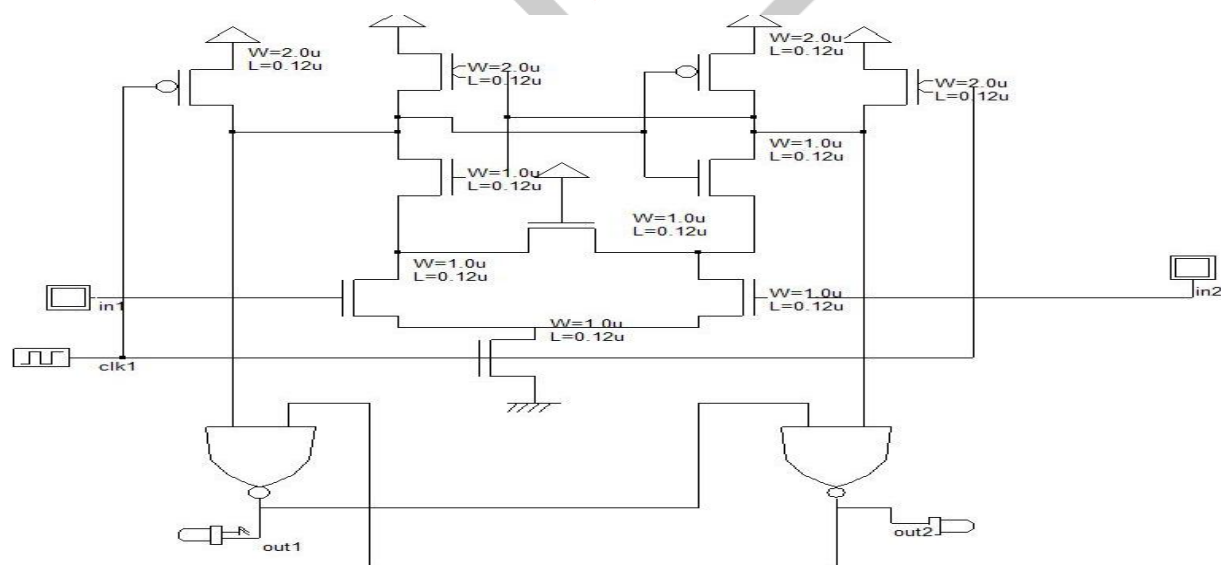|	TYPES	TOTAL NUMBER OF TRANSISTORS	NUMBER OF TRANSISTORS CONNECTED TO CLOCK
FLIP-FLOP	POWER PC FLIP-FLOP	16	8
	SENSE AMPLIFIER BASED FLIP-FLOP	18	3
	ADATIVE COUPLING FLIP-FLOP	22	4

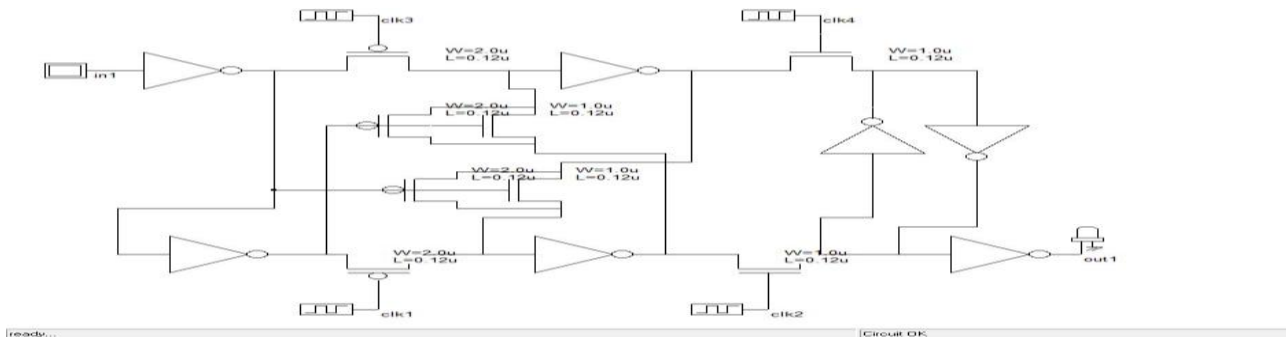Fig.13 Schematic of Sense Amplifier Based Flip Flop

Fig.14 Schematic of Adaptive Coupling Flip Flop

TABLE III. COMPARISON OF PULSED LATCH

PULSED LATCH	WORD LENGTH OF SHIFT REGISTER (256)	SUBSHIFT REGISTERS (K)	CORE AREA	AREA (μM^2)	POWER (MW)
Existing method	256	4	6583	63.2% (occupied)	56.3%
		8	6321	59.0% (occupied)	56.5%
Modified method	256	4	2174	79% (saved)	71%
		8	1483	66% (saved)	80%

V.CONCLUSIONS AND FUTURE WORK

Design of shift register using pulsed latches reduces the area and power efficiently. This method solves the timing problem by the use of multiple non-overlap delayed pulsed clock signals instead of conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shift registers and using additional temporary storage latches. The above work was implemented using Microwind Software. In the previous work consists of 1-bit latch. Hence a 256-bit shift registers with 4-bit sub module, which occupies a core area of $6583\mu m^2$. It consumes 56.3% power and occupies 63.2% area. Similarly using 8-bit sub module, which occupies a core area of $6321\mu m^2$. It consumes 56.5% power and 59% area.

A new method is proposed by modifying the previous approaches. This approach consists of 8-bit latch. 256-bit shift register with 4-bit sub module which occupies a core area of $2174\mu m^2$. It saves 79% area and 71% power. Similarly using 8-bit sub module, which occupies a core area of $1483\mu m^2$. It saves 66% area and 80% power compared to the conventional shift register.

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