Modified SEPIC Converter with High PF Rectifier

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***Abstract*—To overcome the problems of input current ripple operating in DCM, a new a modified version of the SEPIC dc–dc converter used as preregulator operating in discontinuous conduction mode (DCM) at low input voltage is introduced. Only one semiconductor switches are used the proposed rectifier. Hence, the switch voltage reduction increases the converter reliability and a low drain-to-source on-resistance (RDSon) MOSFET can be used depending on the converter specification. The proposed topology operates in discontinuous conduction mode (DCM). The DCM operation has advantage of simple control circuitry. The proposed topology is compared with classical SEPIC preregulator in terms of the power factor and THD.**

***IndexTerms*— discontinuous conduction mode (DCM), high power factor (HPF), single end primary inductor converter (SEPIC)rectifier**

I. INTRODUCTION

single ended primary inductor converter (SEPIC) is a type of DC-DC converter allowing the electrical potential (voltage) at its output to be greater than, less than, or equal to that at its input. The output of the SEPIC is controlled by the duty cycle of the control transistor. The SEPIC converter is similar to a traditional buck-boost converter and cuk converter, but has advantages of having non-inverted output (the output has the same voltage polarity as the input), using a series capacitor to couple energy from the input to the output and the input side inductor can reduce the input current ripple. SEPIC has pulsating output current. Since the SEPIC converter transfers all its energy via the series capacitor, the capacitor should have high capacitance and current handling capability. SEPIC PFC converter can provide a higher power factor regardless its output voltage due to its step up/down function. SEPIC found applications of where the output voltage can be above or below than that of the input voltage. So the SEPICs are useful in applications in which a battery voltage can be above and below that of the regulator's intended output. And also it is applicable for uninterrupted power supplies, dc motors, power factor correction etc.

The usual solution for the implementation of a high power factor (HPF) preregulator for a low-output power application is to use a boost converter operating in discontinuous conduction mode (DCM) [1], [2]. This is a simple and cost-effective solution because the design of the rectifier in DCM allows the converter to operate as a voltage follower, where the input current naturally follows the input voltage profile without the use of a current-control loop.

The classical SEPIC converter, shown in Fig. 1, presents a step-up/step-down static gain and usually is used as an HPF preregulator in applications where the output voltage must be lower than the peak of the ac input voltage [3], [4]. The implementation of the preregulator using the classical SEPIC converter in DCM presents two additional operation characteristics. Firstly,the converter operates as a voltage follower when designed in DCM with a low value for the inductor L2 and using a high. value for the inductor L1 , but the input current presents a low current ripple just as a boost rectifier operating in CCM with current-control loop [3].

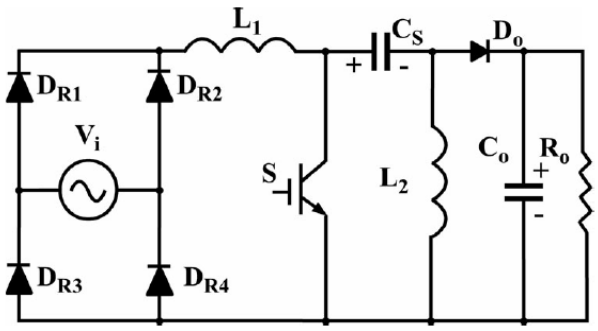

Fig.1.Bridged SEPIC Rectifier

Consequently, the Lf –Cf filter used in the boost converter input operating in DCM is not necessary using the SEPIC converter operating in DCM. Therefore, the number of components for both converters operating in DCM is equal. However, in a practical application, an electromagnetic interference (EMI) filter is necessary as in any rectifier topology. The second important characteristic using the SEPIC converter in DCM is that the input current follows the input voltage waveform without input current distortion. The third-harmonic distortion is not presented because the inductor L2 is demagnetized with the output voltageThe lowest switch voltage level is presented by the modified SEPIC topology.The modified SEPIC converter operates as a voltage follower and the input current presents low current ripple such as a classical SEPIC converter, designing the converter in DCM and using a low value for the inductor L2 and a high value for the inductor L1.

I. PROPOSED SEPIC PREREGULATOR

The modified SEPIC converter used as preregulator operating in DCM is shown in Fig. 3. The main difference from the preregulator is the operation mode and the control system that is composed by only a voltage control loop due to the DCM operation. Also, the non dissipative current snubber used is not necessary because the reverse recovery current of the diodes and the turn-on switching losses operating in CCM are reduced with the DCM operation.

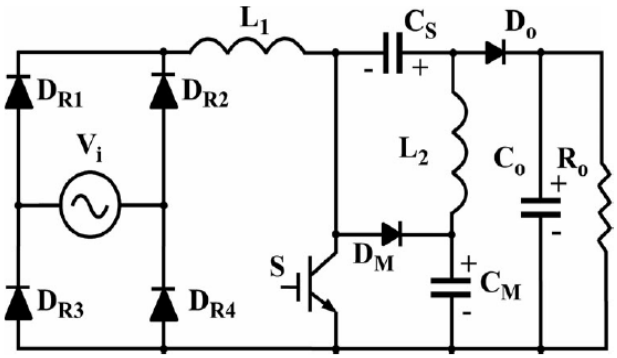

Fig.2. Proposed SEPIC Preregulator.

The modified SEPIC dc–dc converter operating in DCM presents three operation stages. The theoretical analysis is initially developed considering the operation as a dc–dc converter at steady state and all circuit components are considered ideal. The voltages across all capacitors are considered constant during a switching period, as an ideal voltage source. The DCM operation occurs when there is the third operation stage, where the power switch is turned off and the currents in all diodes of the circuit are null. Therefore, the DCM operation occurs when Do and D diodes are blocked before the switch turn-on. The analysis and design procedure is also developed for the operation as a preregulator with a diode bridge at input and an ac input voltage, based on the study as dc–dc converter.

Considering the operation at steady state, the average voltage across the inductors L1 and L2 are null and the sum of the input voltage Vi and capacitor C_s voltage is equal to the capacitor C_M voltage.

The operation stages in DCM are presented as follows:

$$VCM = Vi + VCS \quad \text{.....(1)}$$

II. MODES OF OPERATION

The proposed circuit consists of two symmetrical configurations as shown in Fig. 3 and 4.

1) **First Stage** [$t_\circ - t1$]):

During the conduction of the power switch S, the input inductor stores energy with the input voltage applied across L1 (VL1). The voltage applied across L2 (VL2) is equal to the voltage of capacitor CM minus the voltage of capacitor CS . As presented in (1), this voltage difference is equal to the input voltage. Therefore, inductors L1 and L2 store energy in this operation stage and the same voltage is applied across these inductors. The currents through inductors L1 and L2 increase following (3) and (4), respectively, but since L2 is lower than L1 , the current variation in L2 is higher than in L1 , as presented in the theoretical waveforms shown in Fig. 7. The diodes DM and Do are blocked during this operation stage

$V_{L1} = V_{L2} = Vi$ .....(2)

$\Delta i_{L_1} = \frac{Vi * D}{L_1 * f}$ .....(3)

$\Delta i_{L2} = \frac{Vi * D}{L_2 * f}$ .....(4)

where f is the switching frequency and D is the converter duty cycle.

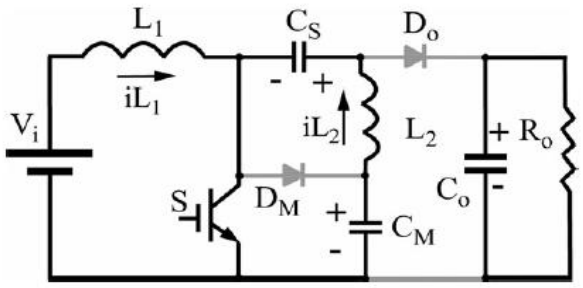

Fig.3. First operation stage

2) **Second Stage** [t1 − t2] (see Fig. 5):

At the instant t1 , switch S is turned off and the energy stored in the input inductor L1 is transferred to the output through the CS capacitor and output diode Do . There is also energy transference to CM capacitor through diode DM and the maximum switch voltage is equal to the CM capacitor voltage. The energy stored in inductor L2 is also transferred to the output and capacitor CS through diodes Do and DM . The voltage applied across L1 is equal to C_M capacitor voltage minus the input voltage and this difference is equal to the C_S capacitor voltage as calculated by (1). The voltage across the inductor L2 is equal to the negative capacitor CS voltage. Thus, the voltage applied across the inductor L1 and L2 are equal to the negative capacitor CS voltage during this operation stage and the inductor current variation is calculated by (6) and (7), respectively. As presented in Fig. 7, the time interval (t2–t1) of the second operation stage is defined as td and is equal to the transference period of the energy stored in inductors L1 and L2 through diodes Do and D_M . When L2 current value becomes equal to L1 current value with the same direction, the currents at diodes Do and D_M becomes null, finishing this operation stage. Therefore, td is the conduction time of diodes D_M and Do , when the energy stored in the inductors L1 and L2 is transferred

$V_{L1} = V_{L2} = -V_{C_S}$ .....(5)

$-\Delta i_{L_1} = \frac{-VC_S * Dt_d}{L_1 * f}$ .....(6)

$-\Delta i_{L_2} = \frac{-VC_S * Dt_d}{L_2 * f}$ .....(7) $Dt_d = \frac{t_d}{T} = t_d * f$ .....(8)

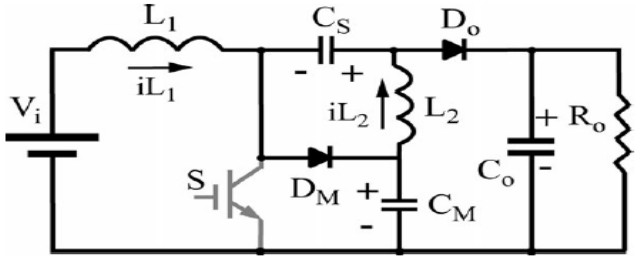

Fig.5. Second operation stage.

3) **Third Stage** [t3 − t4]:

When diodes Do and DM are blocked at the instant t3 , the voltage applied across the inductors L1 and L2 are null, maintaining the inductors currents constant as presented in (9) and (10). The currents through them inductors L1 and L2 present the same value, operating as a freewheeling stage. This operation stage is finished when the power switch is turned on at the instant t4 , returning to the first operation stage

VL1 = VL2 = 0 ..... (9)

ΔiL1 = ΔiL2 = 0 ..... (10)

The main theoretical waveforms are presented in Fig. 7. The switch turn-on occurs with ZCS such as a classical dc–dc converter operating in DCM and the diodes do not present reverse recovery current. The maximum switch voltage is equal to the capacitor CM voltage, and this voltage is lower than the output voltage. The L1 inductor average current is equal to the input

current and the L2 inductor average current is equal to the output current. The average current in the capacitors C_S and C_M are null at steady state; thus, the average current of diodes D_M and D_o are equal to the output current.

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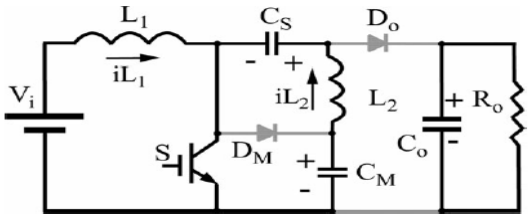

Fig.6. . Third operation stage.

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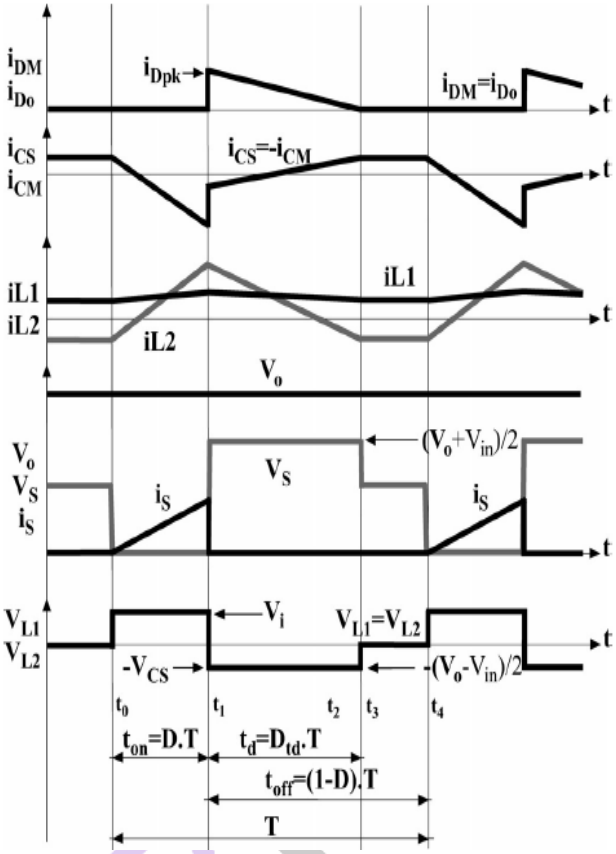

Fig.7. Main theoretical waveforms

SIMULATION AND PARAMETERS USED

Table 1 given below gives the details of the components used for the simulation of the proposed system

Table 1: Values of the components used in the proposed system

Components	**Values**
Inductor L_1 and Inductor L_2	1.77mH and 312.6 µH
Capacitor C_m,	804.1nF
Capacitor C_s	804.1nF
Capacitor C_0	1000µF

III. SIMULATION RESULTS

To verify the input current ripple free condition of the proposed converter, first simulate the conventional converter that is, the converter which does not having auxiliary circuit. Both the converters are simulated by using Matlab/Simulink with simulation parameters . Here input current waveform of both the proposed converter is only compared with the conventional converter .. The converters are designed to get an output voltage of 102V and the power is 30W.

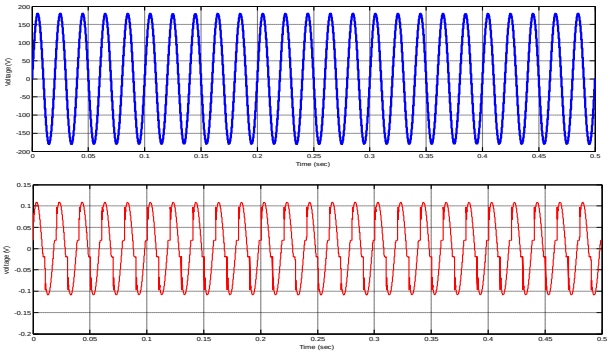

Fig.8. Input voltage and current of conventional SEPIC converter.

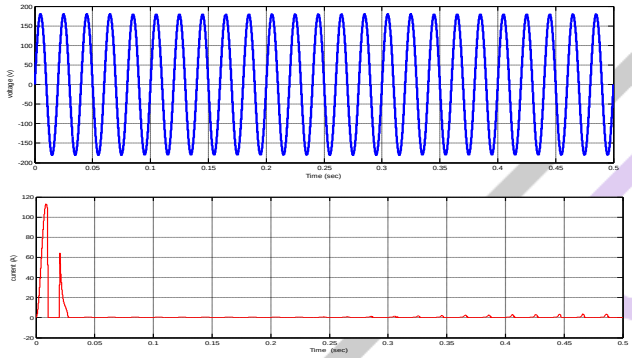

Fig.9. Input voltage and current of modified SEPIC converter.

The output voltage and current waveforms for the conventional SEPIC converter and modified SEPIC converter is shown below in fig.8 and fig.9.

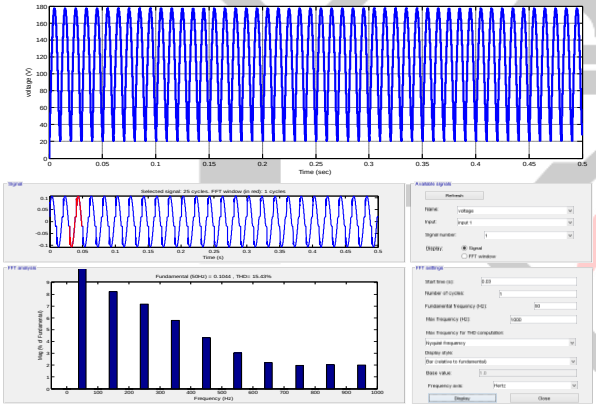

Fig.11. Output voltage and THD of conentional SEPIC converter

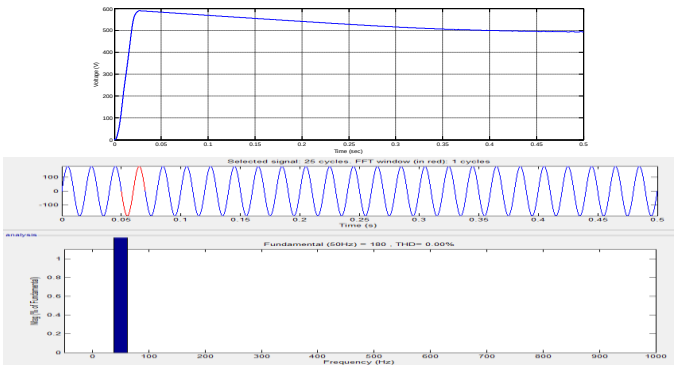

Fig.12. Output voltage and THD of proposed SEPIC converter

The figure shows the input current THD of the proposed circuit.. From the spectrum, it can be analyse that the value of THD is minimum. The input current ripple of the proposed converter is reduced as compared to the conventional circuit so the THD is reduced. So by reducing the THD of the input current, the power factor can be increased.

IV. CONCLUSION

The theoretical and experimental analysis of the modified SEPIC converter used as preregulator operating in DCM is proposed. This converter presents low input current ripple operating in DCM and the switch and diodes voltages are lower than the output voltage. The switch voltage reduction increases the converter reliability and a lower RDSon MOSFET can be used depending on the converter specification. The power factor is higher than 0.998 with the third harmonic reduction in all input voltage range.

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