Design and Simulation of Junctionless Double Gate Graphene FET

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***Abstract*--This paper presents the design and simulation of junctionless double gate graphene FET. This design uses the new materials which have high K. Without suffering serious short channel effects, the designed JL DG graphene device shows excellent characteristics. The designed device shows reduced leakage current, Small SS, high I_{ON}/I_{OFF}. The results obtained show the improvement in the transistor performance for certain parameters.**

Keywords: **Junctionless Double gate FET, Graphene, high-k materials, leakage current, short channel effects, SS.**

I. INTRODUCTION

Recently, junctionless field-effect transistors have become a promising candidate to overcome the limitations of device scaling. These transistors have superior control of short channel effects. A large number of studies focus on sub 10nm devices. Among these devices, the JLFET has more advantages over the conventional inversion mode FETs. These advantages include ease of fabrication, relieving the limitation of thermal budget owing to no source/drain junctions and high immunity to surface scattering.

SCE improvement has become extremely difficult with the CMOS technology scaling for the conventional technology. For this, multi-gate and junctionless FETs are very well known. By using multi-gate structure, there will be ease to control the channel.

Figure 1 Junctionless FET: emerging post CMOS devices

In this paper, the double gate is considered because of its advantages such as: the increase of current provided by this device, for the same channel length, high I_{ON}/I_{OFF}. This double gate FET is wise choice in place of BULK MOSFETs. In this device, both the gate are placed in symmetry covering the channel which are present at the opposite of each other. Moreover, both the gates are connected to the same potential and they have same dimensions.

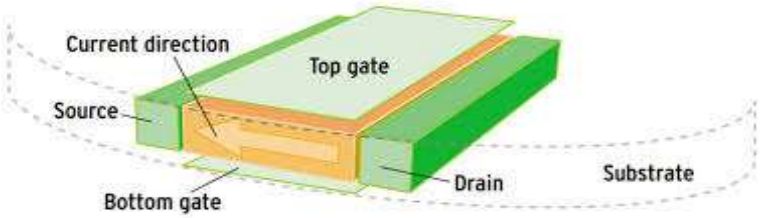

Figure 2 Simple Double Gate FET

Graphene is a form of carbon consisting of planar sheets which are on atom thick, with the atoms arranged in honeycomb-shaped lattice. Graphene is the strongest and thinnest material and it is a super conductor of heat and electricity. Graphene can be used in transistors, semiconductors. The graphene devices are much faster than existing Si devices.

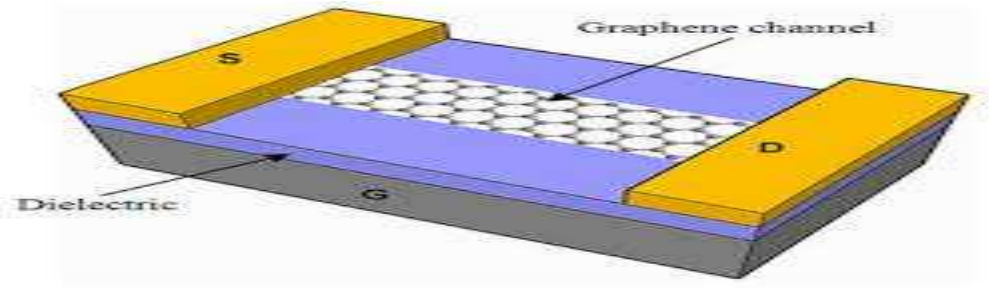

Figure 3 Graphene FET

In this paper, by combining all the above, we proposed junctionless double gate graphene FET. We use high-k materials in this device.

The rest of the paper is organized as follows: Device structure and its simulation is discussed in section II, simulation results are discussed in section III, followed by conclusion in section IV and future scope in section V.

II. DEVICE DESIGN AND SIMULATION

This paper presents the junctinless double gate graphene FET. Here, high-k materials are used to reduce the leakage current and to increase the performance of the device. Some of the high-k materials used as gates are HfO_2, ZrO_2, and TiO_2. By using these materials, the performance of the device has been improved.

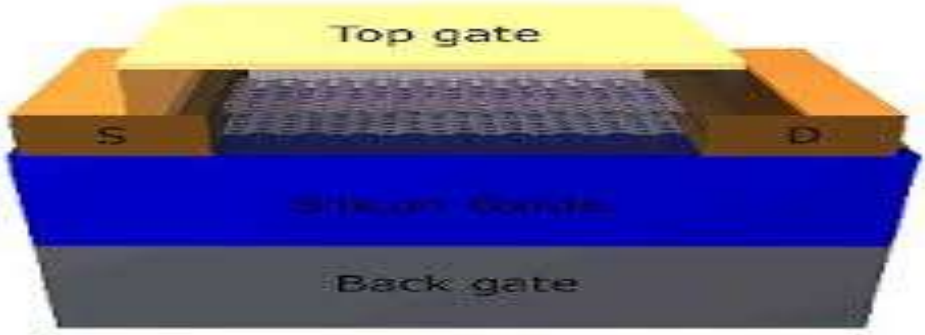

Figure 4 Junctionless Double Gate Graphene FET

Here, graphene material which is the emerging material is considered as the channel. This material is the thinnest and the strongest of all the materials. This is placed above the substrate. With the use of this material in the device, the speed of the device is increased and the device can be used for high frequency applications.

Table 1 High-K Dielectric materials and specifications

	SiO_2	HfO_2	ZrO_2	TiO_2
Relative dielectric	3.90	25	24	80
Specific Heat(j/kg k)	7.09E+02	2.61E+02	4.50E+02	6.90E+02
Thermal conductivity(W/mk)	1.38	22	2	7.4
Electrical conductivity(S/m)	1.00E-15	1.00E-12	3.16E-11	1.00E-13
Density(kg/m^3)	2.2.E	9.68E	5.68E	4.95E+03

In the device, the substrate is taken as SiO_2 and then a graphene channel is taken above the substrate. Different materials such as Si, Al, SiGe, Cu can be considered for source and drain. These materials can also be taken for source, drain and gate metals. High- k materials HfO_2 and ZrO_2 are considered for gates and all these materials can be changed and results can be obtained. With the use of these, the leakage current in the device is reduced.

The Sub-threshold swing (SS) of a device is defined as the change in gate voltage which must be applied in order to create a one decade increase in the output current.

I_{ON}/I_{OFF} is the figure of merit, for having high performance(high I_{ON}) and low leakage power(less I_{OFF}). This device exhibits better I_{ON}/I_{OFF}.

III RESULTS AND DISCUSSION

The characteristics of the junctionless double gate graphene FET were simulated using the open source 2DCC TCAD simulator by varying the device parameters. The device parameters used are: channel length L= 25nm, Si thickness t_{si}=20nm, equivalent gate oxide thickness t_{ox}=5nm, L_{sd} =10nm, doping concentration of the source and drain contact regions N_D= $10^{20}cm^3$. The I_d vs V_d and I_d vs V_g characetistics of the device is studied and also the impact of high- K materials on the device is also studied.

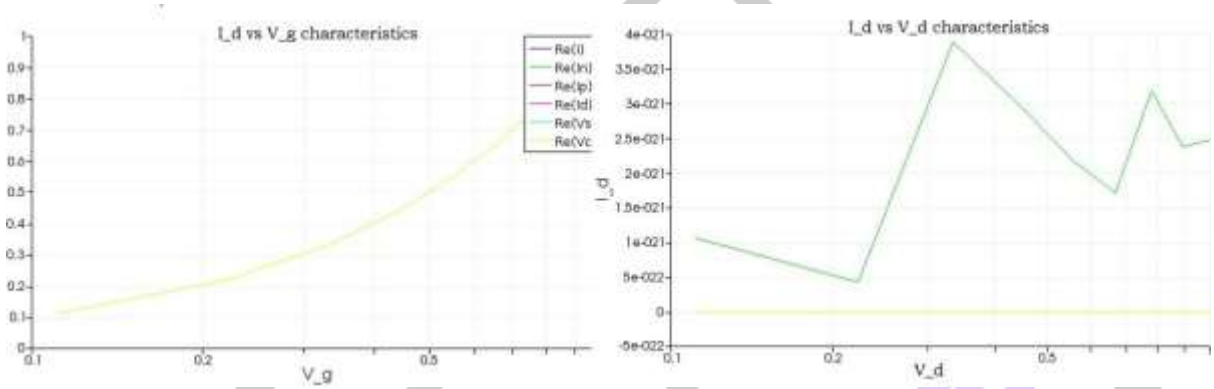

Figure 5 I_d-V_g and I_d-V_d of JL DG Graphene FET (With gate HfO_2/ ZrO_2, t_{ox}=5nm, L_{sd} =10nm and N_D= $10^{20}cm^3$)

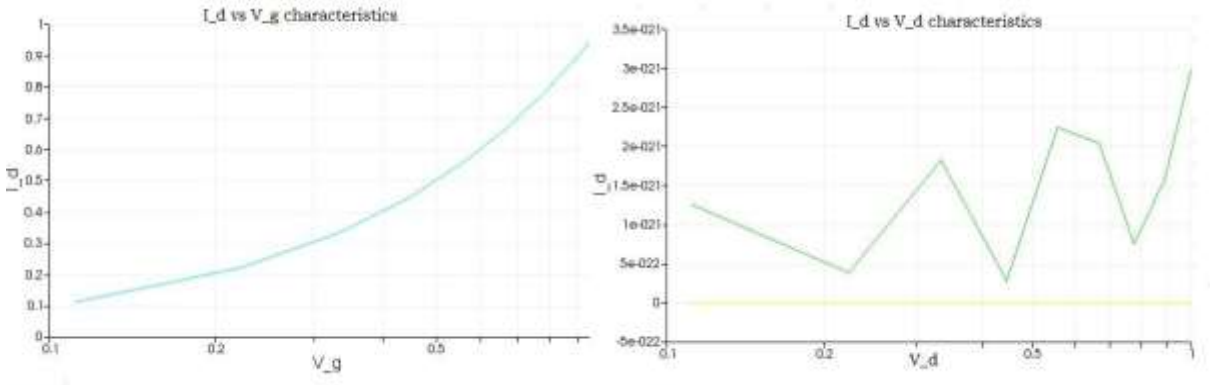

Figure 6 I_d-V_g and I_d-V_d of JL DG Graphene FET (With gate TiO_2, t_{ox}=5nm, L_{sd} =10nm and N_D= $10^{20}cm^3$)

This device has the smaller S.S close to 100 mV/dec and limited SCEs (DIBL ~ 81mV/V).

It has been observed that this device has the better control, higher drive current, reduced short channel effects, reduced leakage current and high I_{ON}/ I_{OFF}(>10^6).

Table 2 Comparison of I_{ON}/I_{OFF} and leakage current		
Materials	I_{ON}/I_{OFF}	Leakage current
High-K materials(HfO_2 ,ZrO_2, TiO_2)	Ratio of >~10^6 for a channel length of 20nm	Very high reduction of leakage current
SiO_2	Ratio of ~10^3 for channel length of 20nm	low reduction of leakage current

IV. CONCLUSION

Junctionless Double Gate Graphene FET is designed and simulated in this paper. In this device, the high- K materials are used such as HfO_2, ZrO_2, TiO_2. By these materials, the performance of the device is improved. An emerging electronic material, graphene is considered as the channel in the design. The device performance is analyzed by using the high- K dielectric materials and found better controllability, reduced leakage current, high drive current and high I_{ON}/I_{OFF}(~>10^6) with the channel length of 20nm.

V. FUTURE SCOPE

In this paper, we used an emerging electronic material, graphene. This material provides promising properties for future CMOS technologies. With its unique properties, it can be the successor of Si. For production of high speed electronic devices in future, graphene can be highly used. As Si devices are running out of ways to increase performance and low power consumption, graphene can completely replace it in the future.

REFERENCES

[1] Tung-Yu-Liu1, Fu-Ming Pan1, and Jeng-Tzong Sheu**, "Characteristics of Gate-all-around Junctionless Polysilicon Nanowire Transistors,"** *Journal of The Electron Devices Society*, Volume 3, No. 5, September 2015.

[2] Lun-Chun chen, Mu-Shih, Ko-wei Lin, Min-Hsin Wu, and Yung-Chun-Wu, "**Junctionless Poly-Si Nanowire FET with Gated Raised S/D,"** *Journal of The Electron Devices Society*, Volume , No. 2, March 2016.

[3] Kian-Hui Goh, Sachin Yadav, Kain Lu Low, Gengchiau Liang, Xiao Gong, and Yee-Chia Yeo, "**Gate-all-around Junctionless Nanowire FET with Tapered S/D Structure,"** *IEEE Transactions on Electron Devices*, Volume 63, Issue: 3, March 2016.

[4] Tao Wang, Liang Lou, and Chengkuo Lee, **"A Junctionless Gate-all-around Si Nanowire FET of High Linearity and its Potential Applications,"** *IEEE Electron Device Letters*, Volume 34, No.4, April 2013.

[5] Sindhu Ramaswamy and Mamidala Jagadesh Kumar, **"Raised Source/Drain Dopingless Junctionless AccumulationMode FET: Design and Analysis,"** *IEEE Transactions on Electron Devices*, Volume 63, Issue: 11, November 2016.

[6] Jae Hur, Dong-Il Moon, Ji-Min Choi, Myeong-LokSeol, Ui-SikJeong, Chang-Hoon Jeon, and Yang-Kyu Choi, "**A Core Compact Model for Multiple-Gate Junctionless FETs**" *IEEE Transactions on Electron Devices* , Volume 62, Issue 7,2015, pp. 2285 - 2291.

[7] Farzan Jazaeri, Lucian Barbut, and Jean-Michel Sallese, **" Modeling Asymmetric Operation in Double-Gate Junctionless FETs by Means of Symmetric Devices,"** *IEEE Transactions on Electron Devices*, Volume 61, NO. 12, December 2014.

[8] Lucian Barbut, Farzan Jazaeri, Didier Bouvet, and Jean-MichelSallese, **"Transient Off-Current in Junctionless FETs,"** *IEEE Transactions on Electron Devices*, Volume 60, NO. 6, June 2013.

[9] Byeong-Woon Hwang, Ji-Woon Yang, and Seok-Hee Lee, **"Explicit Analytical Current-Voltage Model for Double-Gate Junctionless Transistors,"** *IEEE Transactions on Electron Devices*, Volume 62, NO. 1, January 2015.

[10] Jean-Michel Sallese, Nicolas Chevillon, Christophe Lallement, Benjamin Iniguez, and Fabien Pregaldiny, **"Charge-Based Modeling of Junctionless Double-Gate FETs,"** *IEEE Transactions on Electron Devices*, Volume 58, NO. 8, August 2011.

[11] Jorge-Daniel Aguirre-Morales, Sebastian Fregonese, Chhandak Mukherjee, Cristell Maneux, and Thomas Zimmer, "**An Accurate Physics Based Compact Model for Dual-Gate Bilayer Graphene FETs,"** *IEEE Transactions on Electron Devices*, Volume 62, NO. 12, December 2015.

[12] Saul Rodriguez, Sam Vaziri, Anderson Smith, Sebastian Fregonese Mikael Ostling, Max C. Lemme, and Ana Rusu, **"A Comprehensive Graphene FET model for Circuit Design,"** *IEEE Transactions on Electron Devices*, Volume 61, NO. 4, April 2014.

[13] Saungeun Park, Seung Heon Shin, Maruthi N. Yogeesh, Alvin L. Lee, Somayyeh Rahimi, and Deji Akinwande, **"Extremely High Frequency Flexible Graphene Thin Film Transistors,"** *IEEE Electron Device Letters*, Volume 37, Issue: 4, April 2016.

[14] Ime J. Umoh, Tom J. Kazmierski, and Bashir Al-Hashimi, **"A Dual-Gate Graphene FET Model for Circuit Simulation – SPICE Implementation,"** *IEEE Transactions on NanoTechnology*, Volume 12, Issue: 3, May 2013.

[15] Akira Satou, Gen Tamamushi, Kenta Sugawara, Junki Mitsushio, Victor Ryzhii, and Taiichi Otsuji, **"A Fitting Model for Asymmetric I-V Characteristics of Graphene FETs for Extracton of Intrinsic Mobilities,"** *IEEE Transactions on Electron Devices*, Volume 63, NO. 8, August 2016.