

# Bridgeless Power Factor Correction SEPIC Converter

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**Abstract**— This project aims at developing a new single-phase ac dc bridgeless SEPIC converter at low input voltage in order to improve the power factor. The SEPIC converter has non-inverting output. The two semiconductor switches used in the proposed rectifier, replaces the input bridge rectifier. Hence, the conduction losses are less compared to the conventional full bridge topology. The proposed topology operates in discontinuous conduction mode (DCM). The DCM operation has advantage of simple control circuitry. The proposed topology is compared with bridged full-bridge SEPIC rectifier in terms of the power factor.

**Index Terms**— discontinuous conduction mode (DCM), power factor correction (PFC), single end primary inductor converter (SEPIC) rectifier

## INTRODUCTION

Power electronics finds an important place in modern technology being a core of power and energy control. Power supplies with active power factor correction (PFC) techniques are necessary for many types of electronic equipments to meet there harmonic regulations and standards, such as the IEC 61000-3-2 [2]. PFC rectifiers have wide range of application in the industries such as telecommunication and biomedical industries.

The power factor correction topologies so far implemented uses a boost- type circuit configuration because of its lower cost and high efficiency, power factor, and simplicity. Universal input voltage applications, the boost converter suffers from lower efficiency and higher total harmonic distortion at low input voltage. The boost converter has high switch voltage stress which is equal to the output voltage. Some of the practical drawbacks of the boost rectifier are, isolation between the input-output cannot easily be implemented, high inrush of current during start up, and during overload condition there is a lack of current limiting.

The boost converters operating in discontinuous current mode (DCM) have a number of advantages, like inherent PFC function, very simple control, and soft turn-on of the main switch. But, the DCM operation requires a high-quality boost inductor in order to switch extremely high peak ripple currents and voltages. Hence, a more robust input filter is employed to suppress the high-frequency components of the pulsating input current, which increases the overall weight and cost of the rectifier. Several other PFC topologies based on flyback, buck-boost, and Cuk converters were introduced [4]–[10]. However, the main drawback of these topologies is the inverting output.

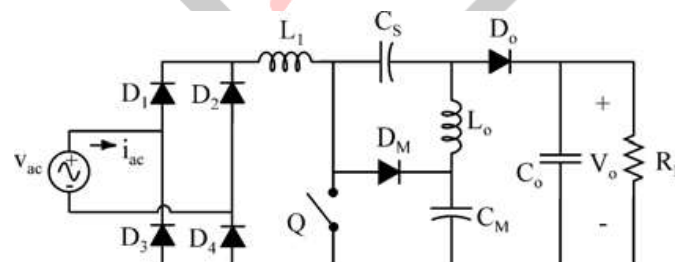


Fig.1. Bridged SEPIC Rectifier [3]

SEPIC is a DC/DC converter topology and it provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. Nowadays electronics equipment requires dc as the input for its operation. So, a converter for ac to dc conversion was found out, which is called bridged SEPIC converter. Fig.1, shows a bridged SEPIC rectifier, which utilizes a full bridge at the input side and results in higher conduction loss as the current flows through at least two bridge diodes at any instant of time. The power factor of this topology has some amount of ripple and is slightly less than unity.

In this paper, a new single-phase ac–dc PFC bridgeless rectifier [1] operating in DCM is introduced. With DCM operation soft turn-on switching and relatively low inrush current can be obtained.

I. BRIDGELESS SEPIC CONVERTER

Fig. 2 shows the proposed bridgeless SEPIC PFC rectifier. With the bridgeless configuration the conduction losses is reduced and the multiplier cell ( $D_1, C_3$  and  $D_2, C_3$ ) increases the gain and reduce the switch voltage stress. The bridgeless SEPIC converter is derived from the bridged SEPIC converter. Bridgeless converter is introduced in order to overcome the drawbacks of bridged converter.

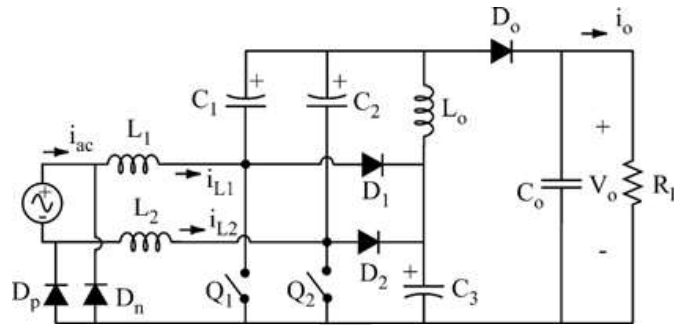


Fig.2. Proposed Bridgeless SEPIC Rectifier.

The proposed circuit has two symmetrical configurations. Each configuration will operate in a half cycle. With the two slow diodes  $D_p$  and  $D_n$ , the output ground is always connected to the terminals of ac mains directly over the whole ac line cycle. Two non-floating switches ( $Q_1$  and  $Q_2$ ) are utilized for the proposed converter. During the positive half-cycle, switch  $Q_1$  is turned ON/OFF [see Fig. 3] and the current flows back to the source through Diode  $D_p$ .

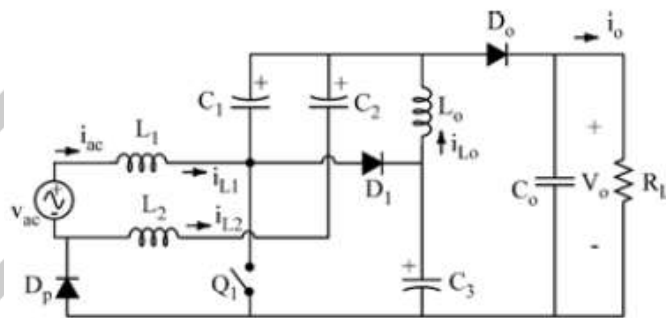


Fig.3. Equivalent Rectifier Circuit during Positive Half Cycle.

During the negative half-cycle, switch  $Q_2$  is switched ON/OFF and the current flowing back through diode  $D_n$  as shown in Fig. 4. Two power switches  $Q_1$  and  $Q_2$  can be driven by the same control signal, which simplifies the control circuitry.

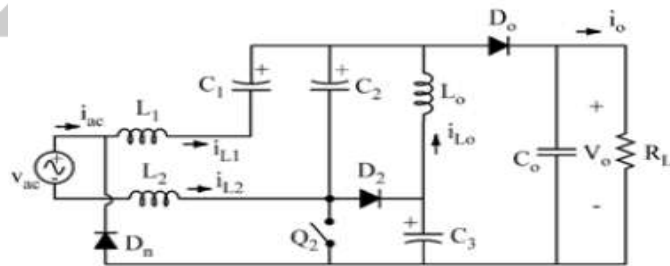


Fig.4. Equivalent Rectifier Circuit during Negative Half-Cycle.

II. MODES OF OPERATION

The proposed circuit consists of two symmetrical configurations as shown in Fig. 3 and 4; the circuit is analyzed for the positive half cycle configuration shown in Fig. 3. Assume that the three inductors are operating in DCM, then the circuit operation during one switching period  $T_s$  in a positive half cycle can be divided into three distinct operating modes as given below.

Mode 1

In this mode, switch  $Q_1$  is turned-on by the control signal and both diodes  $D_1$  and  $D_o$  are reverse biased as shown in Fig. 5. Here, the three-inductor currents increase linearly at a rate proportional to the input voltage  $v_{ac}$

$$\frac{di_{L_n}}{dt} = \frac{v_{ac}}{L_n}, \quad n = 1, 2, o.$$

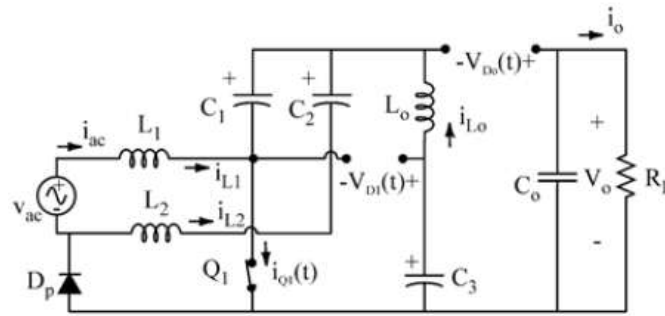


Fig.5. Operation of Proposed Circuit in Mode1

Mode 2

In this subinterval, switch  $Q_1$  is turned-off and both diodes  $D_1$  and  $D_o$  will conduct simultaneously providing a path for the three inductors' currents as shown in Fig. 6. In this mode, the three inductors' currents decrease linearly at a rate proportional to the capacitor  $C_1$  voltage  $V_{C1}$ . This stage ends when the sum of the currents flowing in the inductors adds up to zero, hence diodes  $D_1$  and  $D_o$  are reverse biased

$$\frac{\delta i_{L,n}}{\delta t} = \frac{V_{C1}}{L_{n}}, n = 1, 2, o.$$

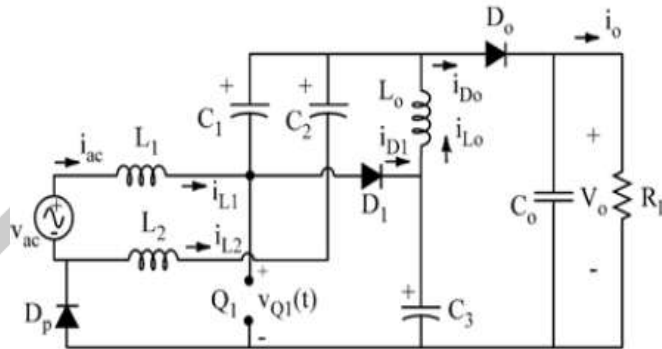


Fig.6. Operation of Proposed circuit in Mode2

Mode 3

In this mode, switch  $Q_1$  remains turned-off while both diodes  $D_1$  and  $D_o$  are reverse biased as illustrated in Fig.7. Diode  $D_p$  provides a path for inductor  $L_0$  current  $i_{L0}$ . The three inductors behave as current sources, which keep the currents constant. So, the voltage across the three inductors is zero. This period ends when switch  $Q_1$  is turned-on initiating the next turn-on of the switching cycle.

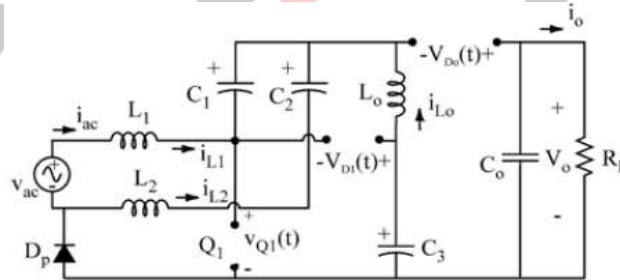


Fig.7. Operation of Proposed circuit in Mode3

Fig. 8 illustrates the theoretical DCM waveforms during one switching period  $T_s$  for the proposed rectifier. The switching frequency ( $f_s$ ) used here is 50kHz.

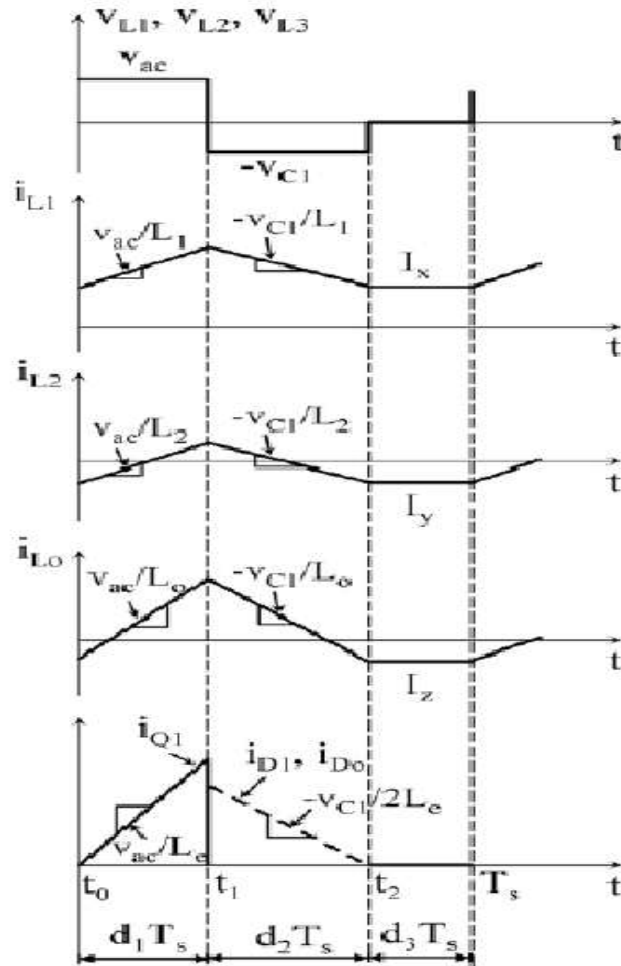


Fig.8. Theoretical DCM Waveform of Proposed System

III. SIMULATION AND PARAMETERS USED

A comparison of the proposed bridgeless SEPIC converter topology with the bridged SEPIC converter topology was performed. The input ac voltage given is 120Vrms. The proposed circuits are designed for getting a 400Vdc output. The load used here is RL load with  $R= 800\Omega$  and  $L=2.5mH$ . Open loop comparison for both the above circuits was performed. Table 1 given below gives the details of the components used for the simulation of the proposed system.

Table 1: Values of the components used in the proposed system

Components	Values
Inductor $L_1$ and Inductor $L_2$	2.2mH
Inductor $L_0$	180 $\mu$ H
Capacitor $C_1, C_2,$ and $C_3$	1.2 $\mu$ F
Capacitor $C_0$	1000 $\mu$ F
Resistor	800 $\Omega$

IV. SIMULATION RESULTS

The simulation results of the bridged SEPIC rectifier and the bridgeless SEPIC converter are given below. The input voltage and current waveforms for the bridged and bridgeless SEPIC converter is shown below in fig.9 and fig.10.

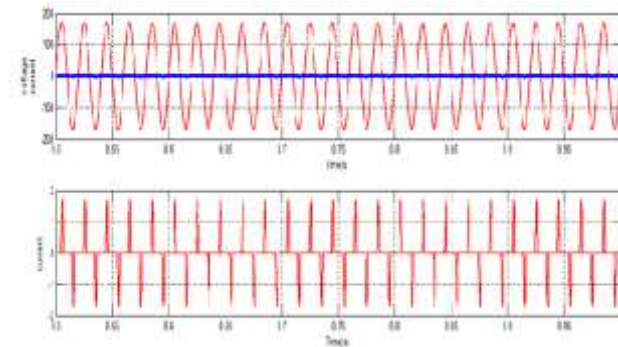


Fig.9. Input voltage and current of bridged SEPIC converter

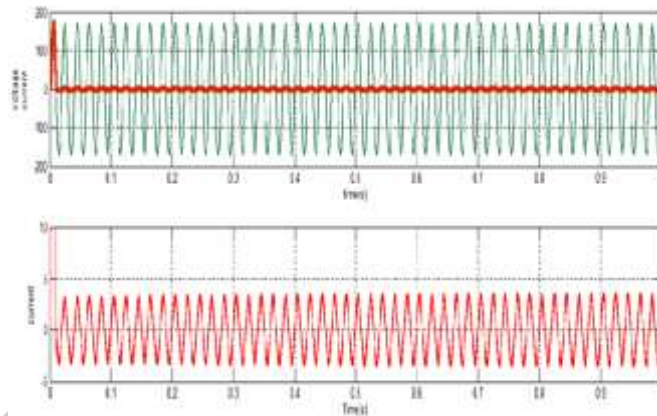


Fig.10. Input voltage and current of bridgeless SEPIC converter

The output voltage and current waveforms for the bridged SEPIC converter and bridgeless SEPIC converter is shown below in fig.11 and fig.12.

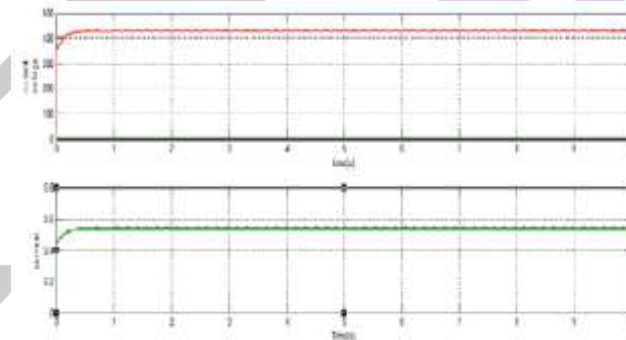


Fig.11. Output voltage and current of bridged SEPIC converter

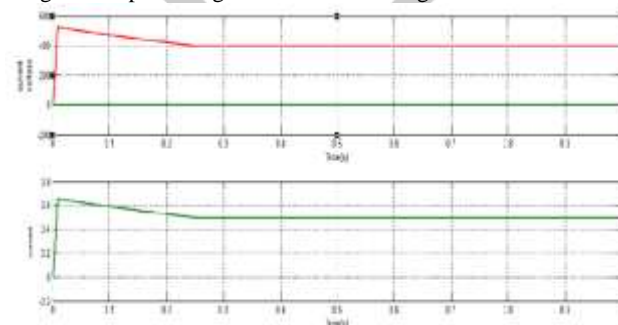


Fig.12. Output voltage and current of bridgeless SEPIC converter

The proposed system is compared with the bridged SEPIC topology for the power factor. It was found that the power factor of the proposed topology is better than the bridged SEPIC converter. Power factor of bridged SEPIC converter and bridgeless SEPIC converter is shown in the fig.13 and fig.14.



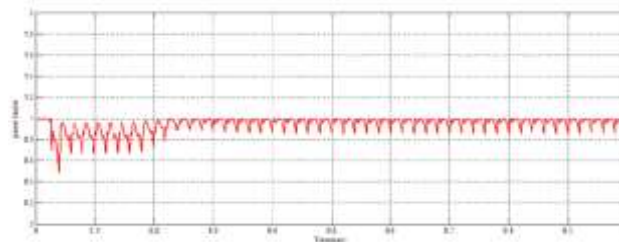


Fig.13. Power factor of bridged SEPIC converter

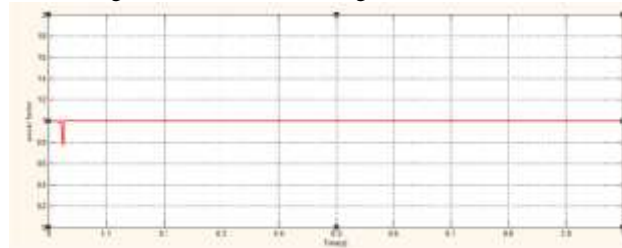


Fig.14. Power factor of bridgeless SEPIC converter

From fig.9, it is found that the input current of bridged SEPIC converter has some distortion. Power factor is defined as the product of displacement power and distortion factor. Hence the power factor of the bridged SEPIC converter is not unity. From fig.10, it is found that the input current of bridgeless SEPIC converter has a little distortion. Hence the power factor is almost unity.

## V. CONCLUSION

The single-phase bridgeless rectifiers with low input current distortion and low conduction losses have been presented and analyzed in this paper. The bridgeless rectifier is derived from the bridged SEPIC converter. Comparing with the bridged SEPIC converter, the bridgeless SEPIC converter has a better power factor. As, the bridgeless topology is used, the conduction losses are reduced. The two power switches in the proposed topology can be driven by the same control signal, which significantly simplifies the control circuitry. Simulation results have been presented to validate the operation of the proposed circuit at open-loop condition.

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