Energy Efficient ALU based on GDI Comparator

[1]Kiran Balu K, [2]Binu Manohar

[1]PG Scholar, [2]Assistant Professor
Dept. of ECE
Mangalam college of engineering
Ettumanoor, Kottayam, Kerala

Abstract— **This paper presents an energy efficient ALU using magnitude comparator designed in GDI(gate diffusion input) technique. The proposed GDI magnitude comparator used ALU has been compared with existing design technologies such as CMOS, Transmission gate logic (TG) and pass transistor logic (PTL). The performance analysis of comparator designed using this technologies is done on the basis of power consumption ,delay and number of transistors using Cadence virtuoso tool and found to be efficient. Based on the performance of GDI comparator in ALU, all blocks of ALU is designed using GDI technology. The simulation results of GDI ALU have shown remarkable performance in terms of power consumption, delay & number of transistors compared to ALU designed using CMOS, TG & PTL. But this GDI ALU suffers from some practical limitation like swing degradation. This limitation can be overcome by modified GDI ALU. Thus proposed GDI ALU can be a viable option for low power application.**

Keywords—ALU, VLSI, Gate Diffusion Input (GDI), CMOS, TG, PTL, Low power, Mod-GDI.

I. INTRODUCTION

Comparators are the basic building block of ALU which are extensively used circuit elements in Very Large Scale Integration (VLSI) systems such as Digital Signal Processing (DSP) processors, microprocessors etc. It is the nucleus of many other operations like sorting, data processing, and decoding instruction. In most of the digital systems, comparators lie in a critical path which influences the overall system performance. Hence, enhancing Comparator performance is becoming an important goal. The performance of comparator can be optimized by proper selection of logic styles. Different logic design styles such as CMOS, PTL, TG technologies can be used. But this techniques have its own drawback such as more number of transistors, more power consumption all. To overcome this problem a new logic style (GDI Technique) has been proposed. GDI technique, Simply uses basic GDI cell consisting of only two transistors and three inputs to implement various complex function. It is proved that GDI technique required lesser number of transistor and low power consumption. Employing fast and efficient GDI comparators in arithmetic logic unit(ALU) will aid in the design of low power high performance system as ALU is one of the main components of a microprocessor. As the number of transistor is reduced in the GDI technique ALU it is obvious that its area is optimized. Apart from this optimized area of ALU the other evident advantage we get is speed. Apparently as the number of transistor used is reduced the operating time is also reduced and operation are done in less time. So our new ALU is also fast in operation as compare to its counterpart

II. LITERATURE SURVEY

The traditional method to implement the comparator is by flattering the logic function directly, but this method is only suitable for the comparator with less number of inputs [1]. When large number of inputs are applied, circuit complexity increases drastically and the operating speed is degraded accordingly. Alternative way to implement the comparator is by using a parallel adder [2]. In this method, the adder has become the major factor for reducing the operating speed. A thousand numbers of transistors are used to increase the speed of adder [3]-[5], Richard [6] proposed a new logic all-n-logic (ANL) to improve the operating speed. Wang [7] used this logic and implemented 64 bit high-speed comparator with two phase clock. It is designed by using six pipeline circuits and each comparison operation through these six pipelines. Even though heavily pipeline is useful to achieve high throughput but it may not be suitable for all applications, such as in the ARM microprocessor [8] which is often needs to execute a comparison instruction with a single clock cycle. Hunag proposed comparator using single clock cycle based on the priority-encoding algorithm [9]. It not only improves the operating speed but also makes circuit more power efficient. Parallel MSB checking algorithm [10] and MUX-based structure [11] was proposed to improve the performance of comparator at the expense of twice the number of transistor.

All of aforementioned works give high performance using dynamic logic. But dynamic logic is not suitable for low power operation as compared to static logic; dynamic activity factor is 0.5 and 0.1 for static logic which is advantageous.

The CMOS technology [12] have been resulted in many circuit design logic style during the last two decade [13] and [14] the various topologies such as conventional CMOS, nMOS pass transistor logic, transmission gates and pseudo nMOS logic style. By using all this logic style 2-Bit magnitude comparator has been implemented by Vandana[15] and Anjuli [16].

The work done in [15] and [16] has shown that the output voltage swing is better in CMOS logic design and transmission gate design, Whereas, Transmission gate logic require more number of transistor as compare to CMOS design. But Pseudo nMOS and PTL logic style requires less no transistor in comparison to CMOS logic style. There is output voltage swing degradation in PTL and Pseudo nMOS logic style.

To overcome this problem a new logic style (GDI Technique) has been proposed by A. Morgenshtein [17]. GDI technique is superior over other design techniques in terms of low power and high speed VLSI design. GDI technique simply uses a basic GDI cell consisting of only two transistors and

three inputs to implement various complex function. The feature of this technique is improved logic level swing, characteristic performance and also allows a simple design of any logic circuit using a small GDI cell. It is proved that GDI technique required lesser number of transistors and low power consumption for the implementation of different logic style, in comparison with CMOS logic style, nMOS Pass transistor Logic and transmission gate [18].

III. CONVENTIONAL DESIGN TECHNOLOGIES OF MAGNITUDE COMPARATOR

Now a days CMOS (Complementary Metal Oxide Semiconductor) logic style is the primary technology in the semiconductor industry. Conventional method such as pass transistor logic, transmission gate logic, etc are also used to construct schematic of magnitude comparator.

A) *CMOS logic*

Fig. 1 show symbol of CMOS inverter consisting of pMOS and nMOS transistors connected at the drain and gate terminal, a supply voltage V DD at the pMOS source terminal and GND connected at the nMOS source terminal, Whereas input (A) is connected to the gate terminals and output (Abar) is connected to the drain terminal.

If input A=0, then pMOS is ON and provides low impedance path from VDD to output (Abar). At that time nMOS is in OFF condition, thus output (A bar) approachs a high level that is VDD. If input A= l, then nMOS is ON and pMOS is in OFF condition, nMOS provide low impedance path from output (Abar) to ground. Therefore, output (Abar) approaches to low level that is 0 V. The substrate pMOS is always connected to VDD and nMOS substrate is always connected to GND. The CMOS inverter provides two important advantages, low static power dissipation and high noise margin.
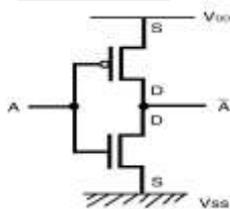

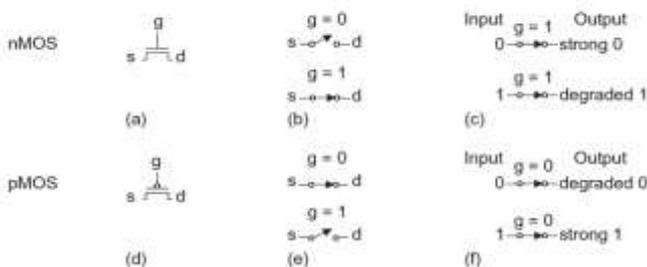
Fig 1: CMOS inverter

B) *Pass transistor logic*

Fig 2: pass transistor logic

When an nMOS or pMOS is used alone as an imperfect switch, we sometimes call it a pass transistor. An nMOS transistor is an almost perfect switch when passing a 0 and thus we say it passes a strong 0. However, the nMOS transistor is imperfect at passing a 1. The high voltage level is somewhat less than *VDD*. A pMOS transistor again has the opposite behavior, passing strong 1s but degraded 0s.
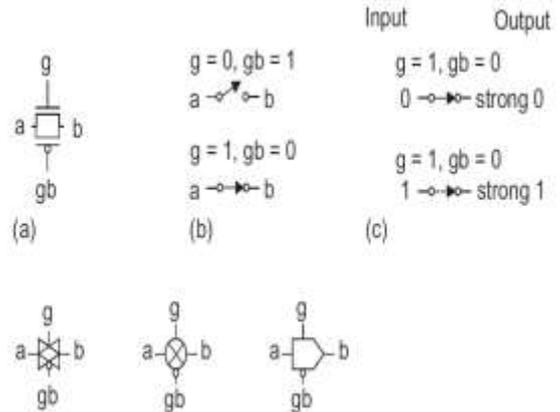
C) *Transmission gate logic*

Fig 3: Transmission gate logic

By combining an nMOS and a pMOS transistor in parallel, we obtain a switch that turns on when a 1 is applied to g in fig. in which 0s and 1s are both passed in an acceptable fashion We term this a transmission gate. Both the control input and its complement are required by the transmission gate. This is called double rail logic. the nMOS transistors only need to pass 0s and the pMOS only pass 1s, so the output is always strongly driven and the levels are never degraded. This is called a fully restored logic gate and simplifies circuit design considerably

IV. PROPOSED GDI TECHNOLOGY

A GDI cell is a new technique for low power combinational circuits. In this approach only two transistors are used to implement a wide range of complex logic functions. The GDI method is based on the use of a simple cell as shown in Fig. 04.
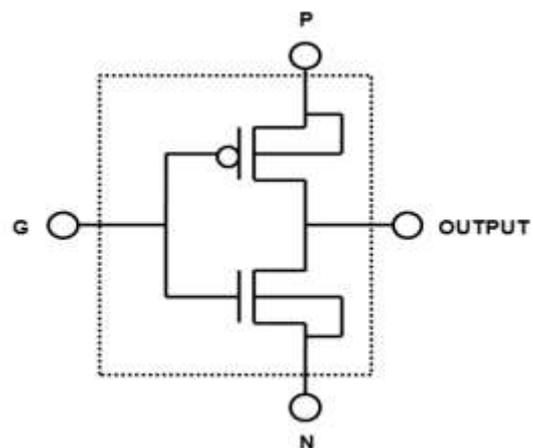

Fig.04. Basic GDI cell

At a first view the basic cell reminds the standard CMOS inverter, but there are some important differences:

1) Gate Diffusion Input (GDI CELL) contains three inputs –G (common gate input of NMOS and PMOS), P(input to the source/drain of PMOS), and N (input to the source/drain of NMOS).

2) The source of PMOS in a GDI cell is not connected to V_{DD} and source of NMOS is not connected to GND . This feature gives GDI cell two extra input pins for use which makes GDI design more flexible.

3) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter .

. A simple change of the input configuration of the simple Gate Diffusion Input (GDI) CELL as shown in figure -15 corresponds to different Boolean functions.

Table I.
Basic functions using GDI CELL

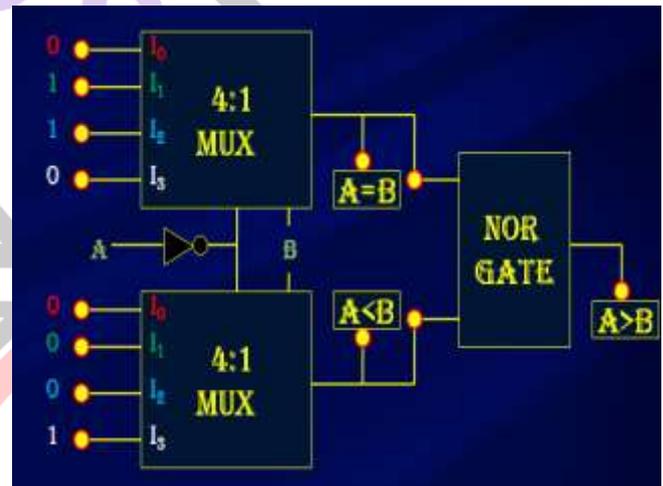| N	P	G	Output	Function
0	1	A	A'	INVERTER
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
B'	B	A	A'B+B'A	XOR
B	B'	A	AB+A'B'	XNOR

Table 2 shows the comparison between GDI and static CMOS design in terms of area count. It can be seen from table 2 that using GDI technique AND, OR, NAND, NOR, MUX can be implemented more efficiently.

Table II.
Comparison of transistor count of GDI and static CMOS

Function	GDI	CMOS
INVERTER	2	2
F1	2	6
F2	2	6
OR	2	6
AND	2	6
MUX	2	12
XOR	4	16
XNOR	4	16
NAND	4	4
NOR	4	4

V. MAGNITUDE COMPARATOR

A magnitude comparator is shown in Fig. 5. It compare two binary numbers A & B. It consists of three outputs. Whenever A equals to B, then output A=B goes high & if A less than B, then output A<B goes high. A greater than B condition is checked using a NOR gate such that when both A=B & A<B goes low, output A>B goes high.

Here Comparator is designed using a multiplexer & NOR gate so that efficiency of GDI technology can be easily highlighted.

Fig.5. Magnitude comparator using mux

VI. DESIGN OF MAGNITUDE COMPARATOR USING EXISTING & PROPOSED DESIGN METHODOLOGY
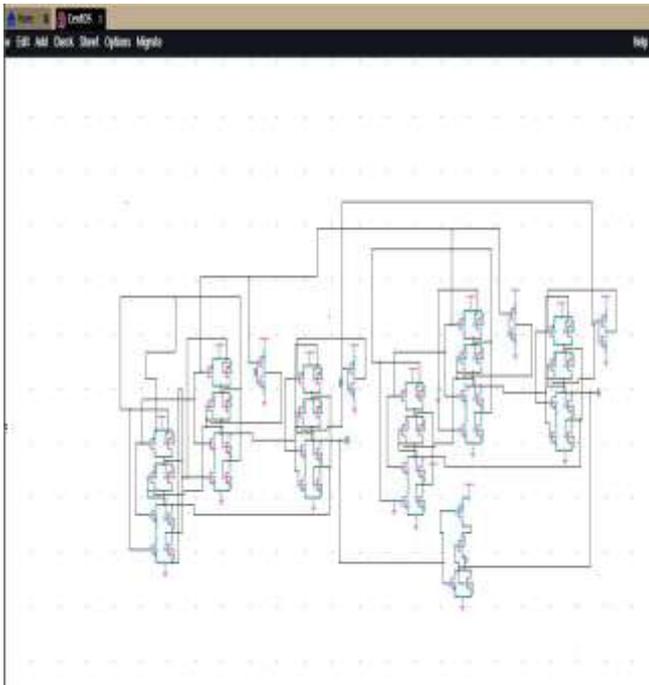
A) *Design & Simulation Results Of Cmos Comparator*
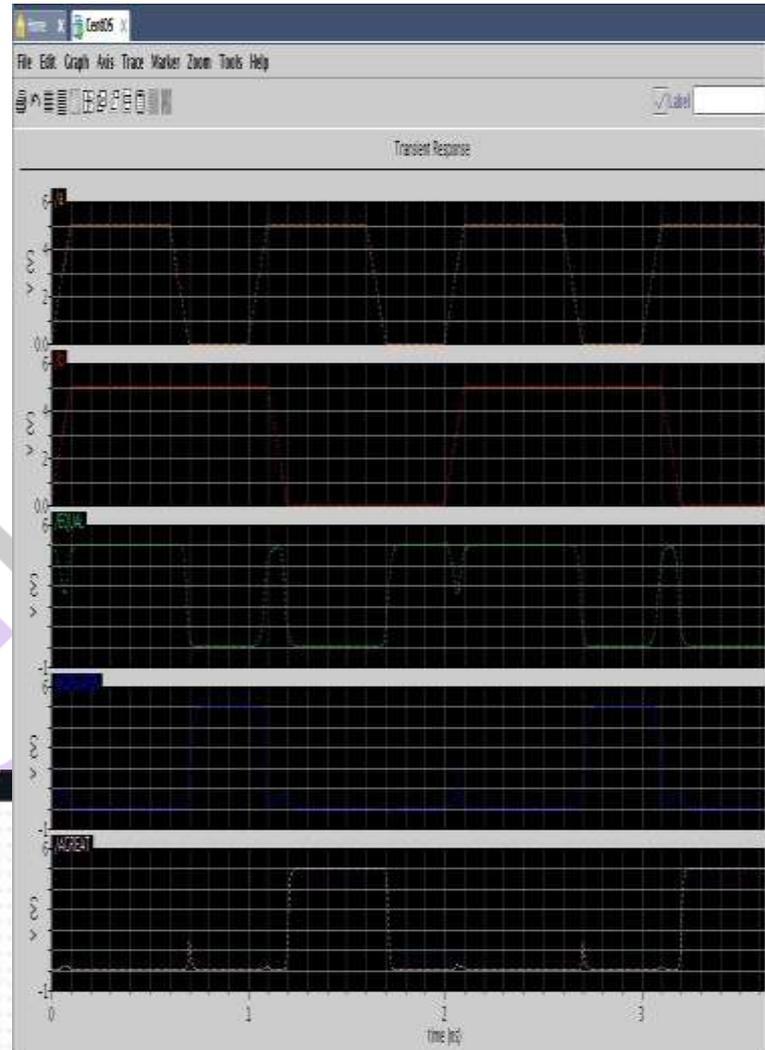
Fig.6. Schematic of CMOS comparator using 2:1 mux

Fig.7. Schematic of CMOS comparator using 2:1 mux block level

Fig.8. waveform of CMOS comparator

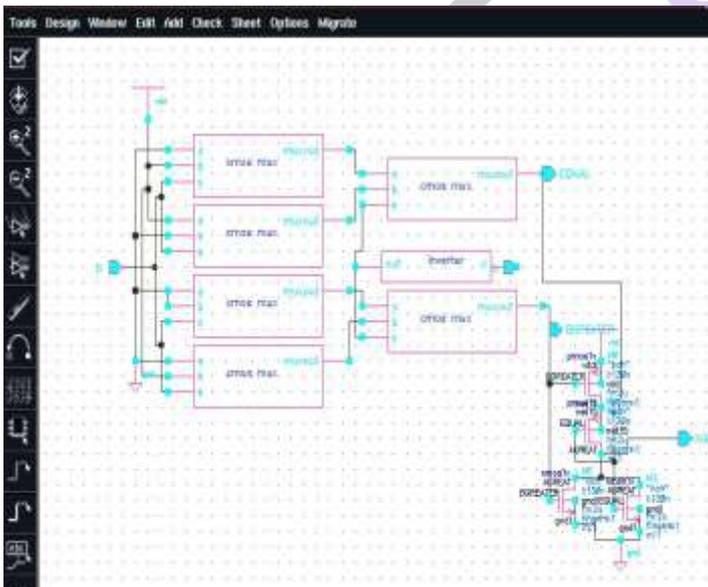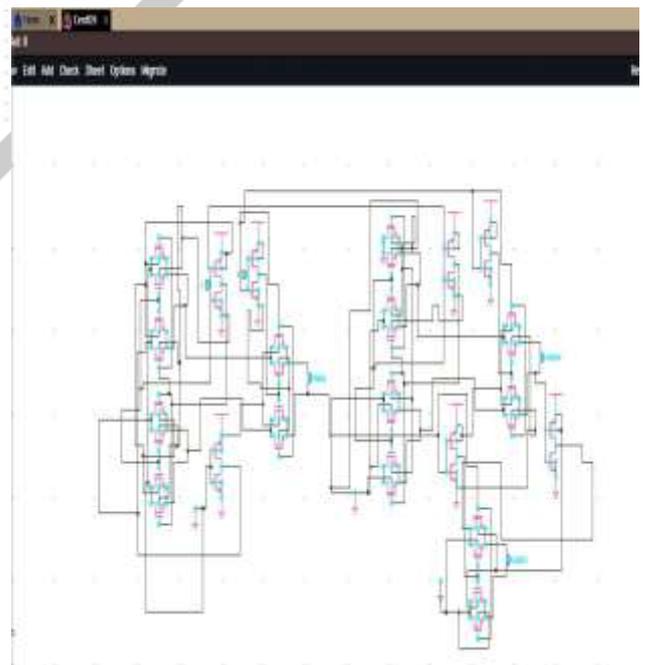B) *Design & Simulation Results Of Transmission gate Comparator*
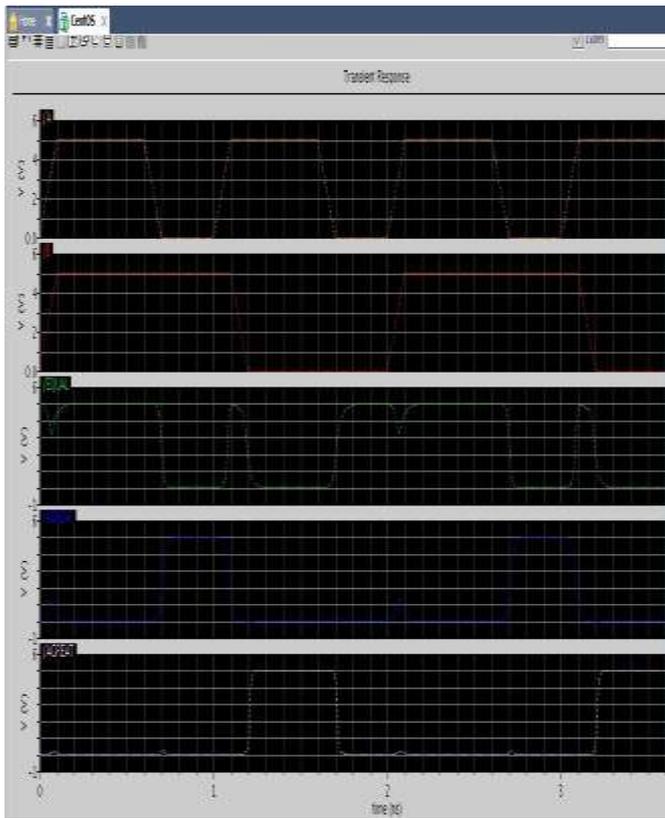

Fig.9. Schematic of Transmission gate comparator
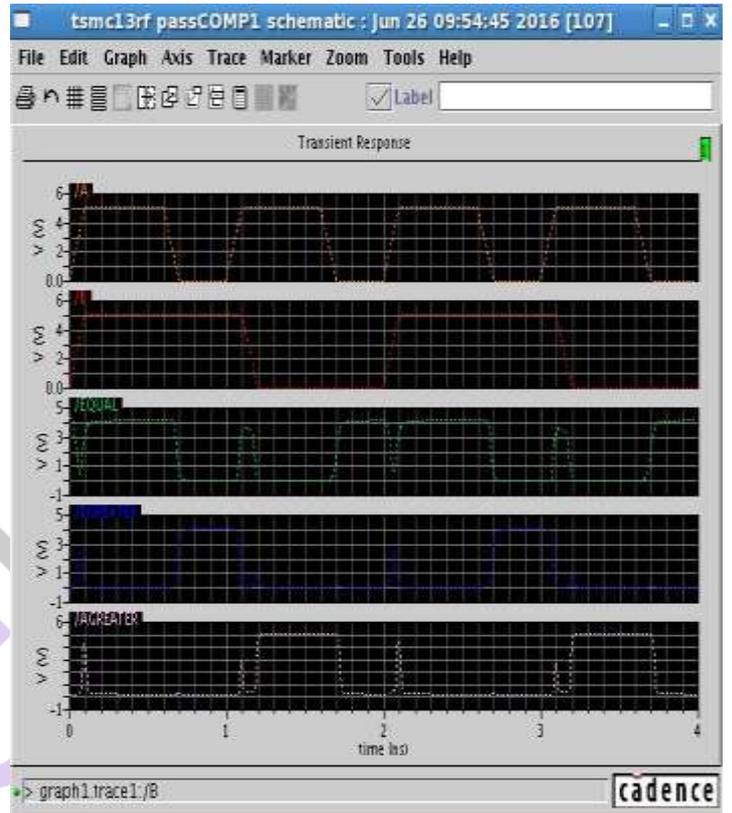
Fig.10. Waveform of Transmission gate comparator

Fig.12. Waveform of pass transistor comparator

C) *Design & Simulation Results Of GDI Comparator*
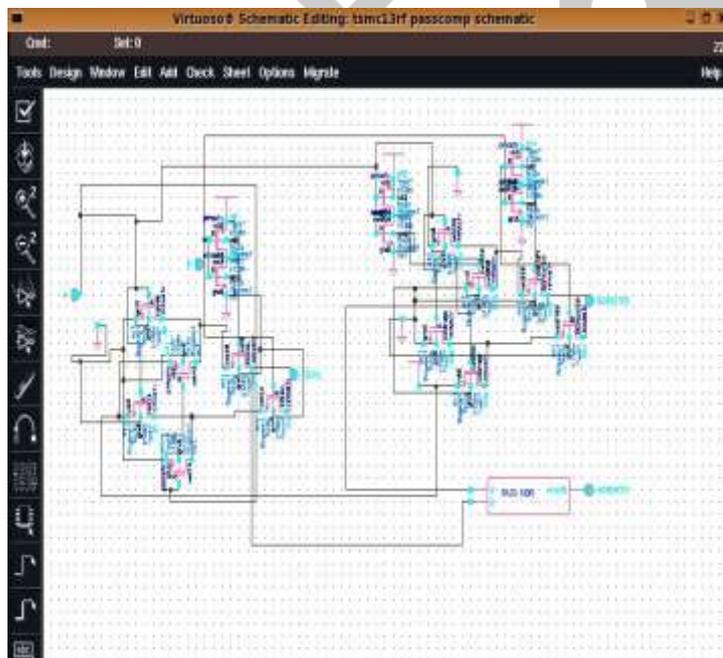
C) *Design & Simulation Results Of Pass transistor Comparator*

Fig.13. Schematic of GDI MUX

Fig.11 Schematic of pass transistor comparator
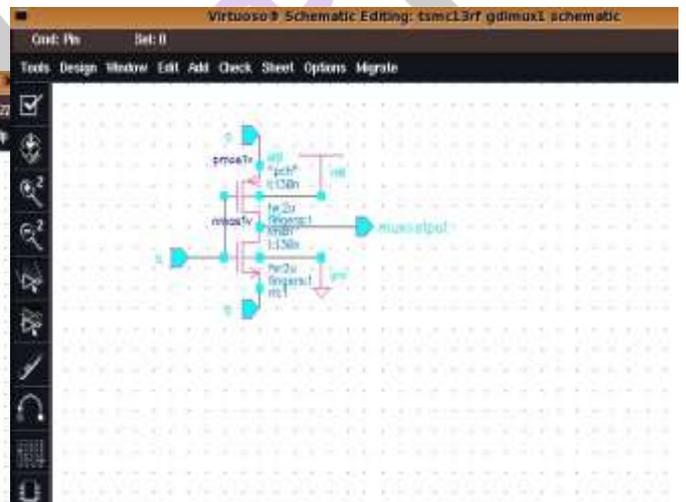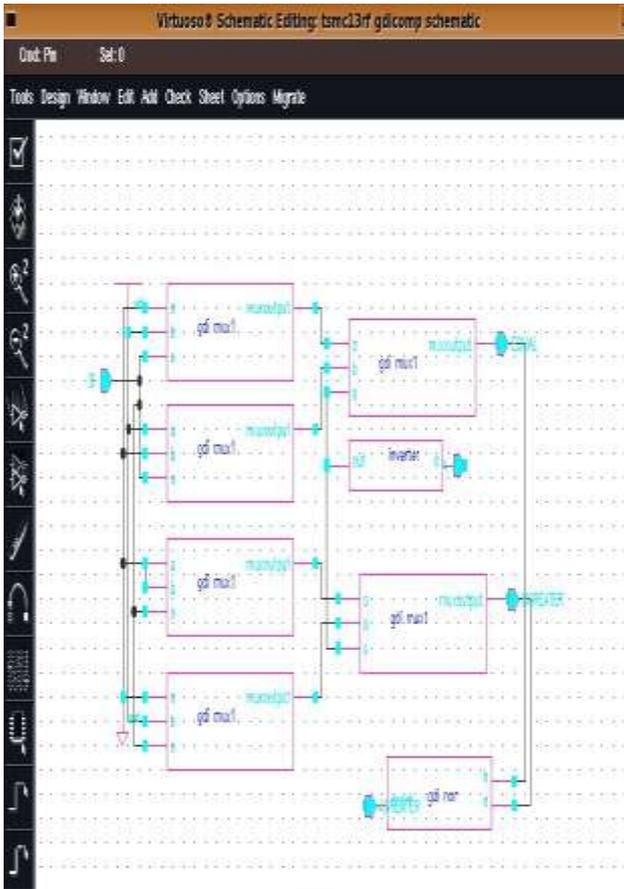
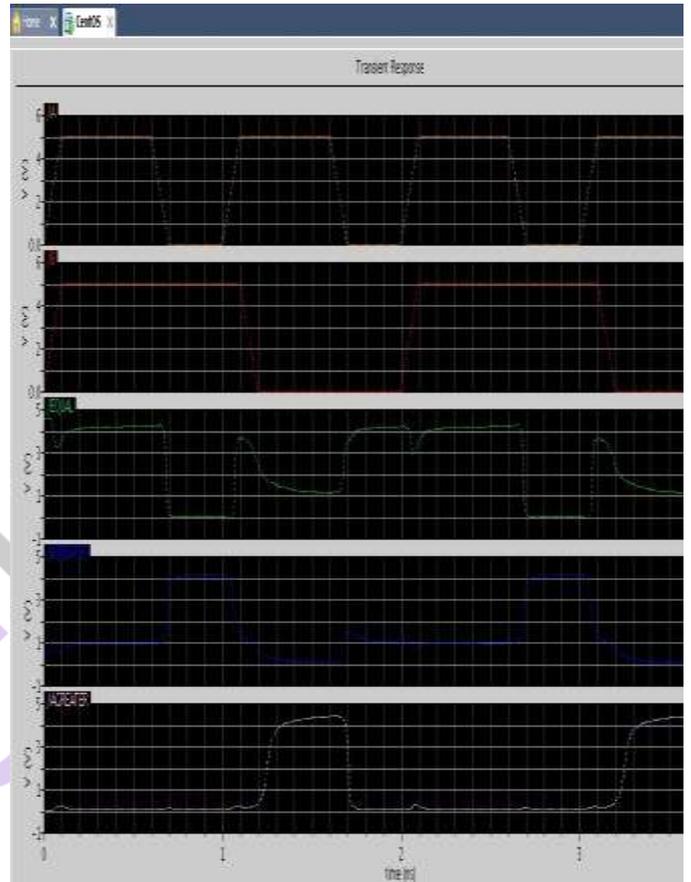Fig.14. Schematic of GDI comparator using GDI MUX

Fig.15. Waveform of GDI comparator

VII. COMPARISON OF EXISTING METHODOLOGIES WITH PROPOSED GDI TECHNIQUE BASED ON DESIGN OF COMPARATOR

Table III.
Comparison of transistor count of GDI and static CMOS

COMPARATOR TECHNOLOGY	AVERAGE POWER DISSIPATION (W)	DELAY (ns)	POWER*DELAY PRODUCT (w*ns)
CMOS	0.01459	4.29	0.0625
TRANSMISSION GATE	0.01303	2.30	0.0299
PASS TRANSISTOR	0.01283	0.508	0.0065
GATE DIFFUSIONINPUT	0.00476	1.352	0.0064

From the analysis it is clear that GDI comparator has low power dissipation compared to existing design techniques. Eventhough there is an increase in delay compared to pass transistor logic, GDI is found to be the lowest power delay product as compared to other techniques. So it is clear that GDI is the efficient technique for designing comparator.

VIII. DRAWBACK OF GDI TECHNIQUE COMPARATOR & SOLUTION

Gate Diffusion Input (GDI) logic style suffers from some practical limitations like swing degradation. The existing GDI gates presented reduced voltage swing at their outputs due to threshold drops, these drops usually cause degradation in performance and increased short circuit power. However, since the GDI circuits were implemented with much less transistors, a significant power overall power reduction was observed, while maintaining minimal performance penalty. These limitations can be overcome by modified gate diffusion input (Mod-GDI).

A) Modified Gdi Technique

Existing GDI gates are modifies by adding an Additional buffer inorder to overcome the drawback of swing degradation. An example of adding buffer to AND gate is shown.
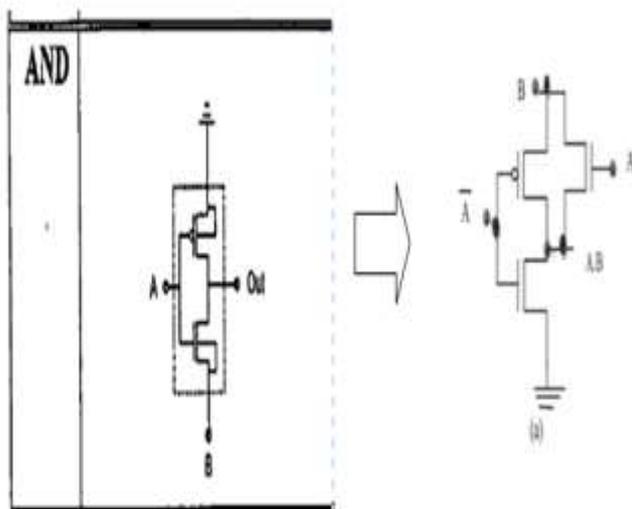

Fig.15. Example of modified GDI technique

Here as PMOS in AND gate gives degraded '0', ' 0' is transmitted through NMOS and a buffer is added parallel to PMOS to transmit strong 0's & 1's.

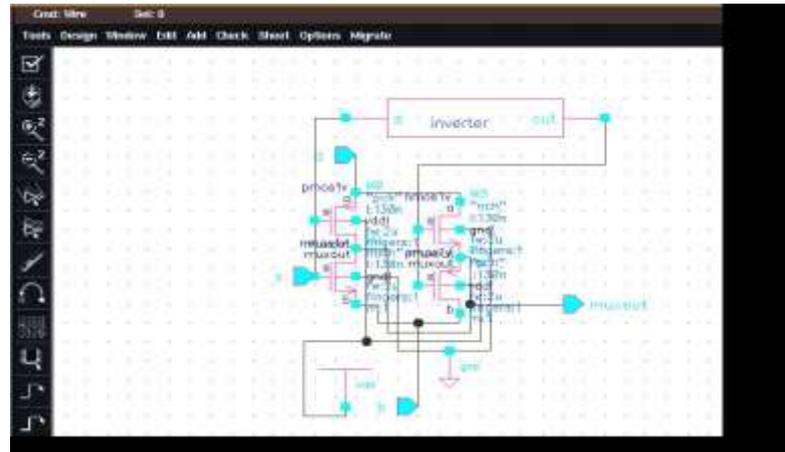*B) Design & Simulation Results Of MOD-GDI Comparator*
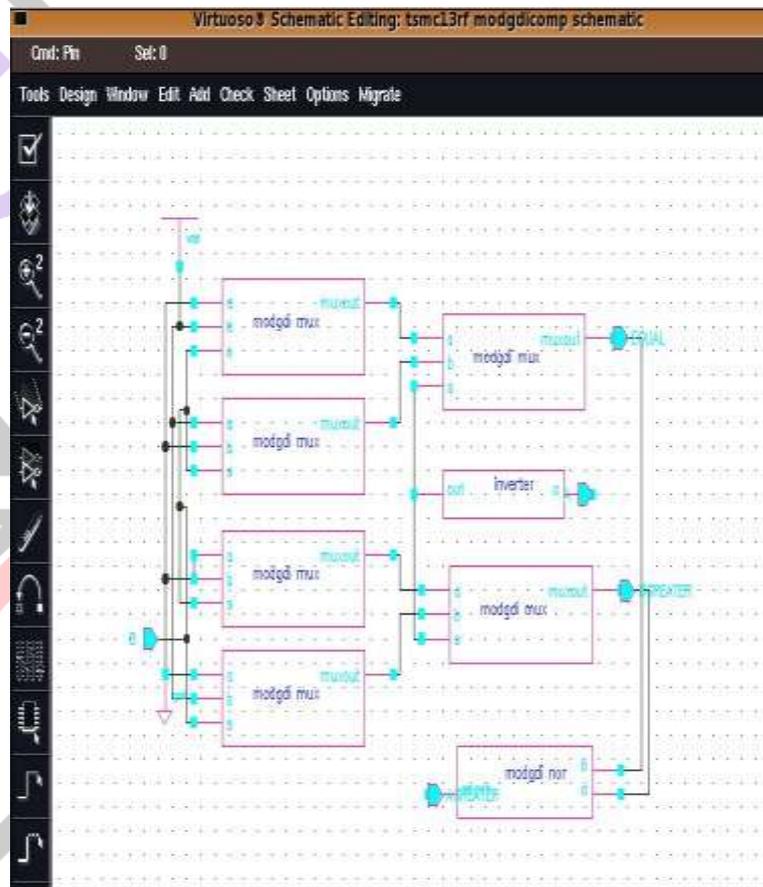

Fig.16. schematic of modified GDI mux

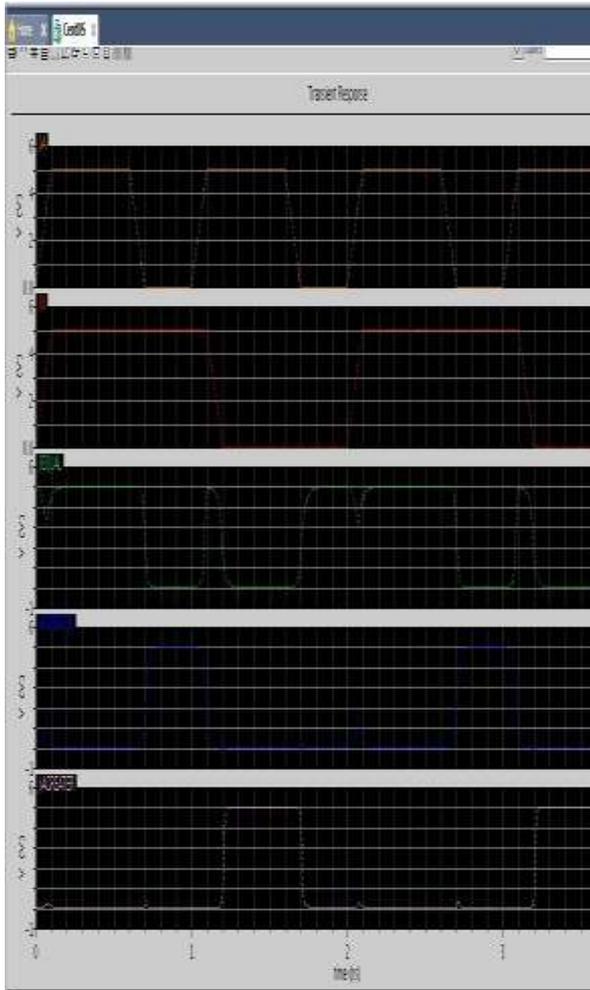Fig.17. schematic of modified GDI comparator using MOD-GDI mux

Fig.18. Waveform of MOD-GDI comparator

C) Comparison Of Existing Methodologies With Proposed Mod- GDI Technique Based On Design Of Comparator

Table.IV.

Comparison Of Existing Methodologies With Proposed Mod- GDI Technique Based On Design Of Comparator

COMPARATOR TECHNOLOGY	AVERAGE POWER DISSIPATION (W)	DELAY (ns)	POWER*DELAY PRODUCT (w*ns)
CMOS	0.01459	4.29	0.0625
TRANSMISSION GATE	0.01303	2.30	0.0299
PASS TRANSISTOR	0.01283	0.508	0.0065
GATE DIFFUSIONINPUT	0.00476	1.352	0.0064
MODIFIED GATE DIFFUSIONINPUT	0.00495	1.195	0.0059

From the analysis, even though there is a small increase in power dissipation compared to GDI technique, MOD-GDI is found to have low delay & low power delay product & also full swing output as compared to other technologies

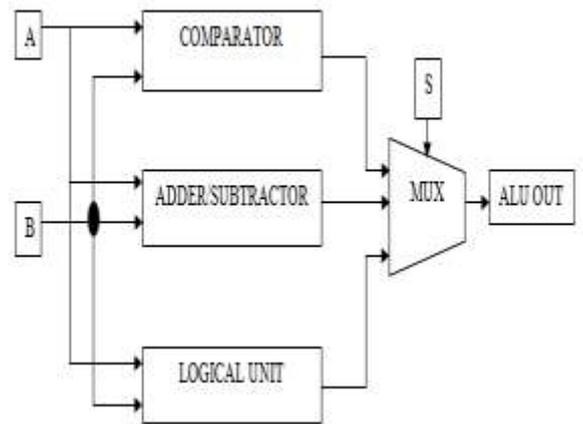## IX.   APPLICATION OF GDI COMPARATOR – ALU

Fig.19. ALU block diagram

Comparators are the basic building block of ALU which are extensively used circuit elements in very large scale integration (vlsi) systems such as digital signal processing (dsp) processors, microprocessors etc.

A processor is a main part of any digital system. And an ALU is one of the main components of a microprocessor. To give a simple analogy, CPU works as a brain to any system & and ALU works as a brain to CPU. So it's a brain of computer's brain. They are consists of fast dynamic logic circuits and have carefully optimized structures. Of total power consumption in any processor, CPU accounts a significant portion of it. ALU also contribute to one of the highest power density locations on the processor, as it is clocked at the highest speed and is busy mostly all the time which results in thermal hotspots and sharp temperature gradients within the execution core.

Therefore , this motivate us strongly for a energy efficient ALU designs that satisfy the high performance requirements, while reducing peak and average power dissipation. Basically ALU is a combinational circuit that performs arithmetic and logical operations on a pair of n bit operands.

So ALU designed using GDI comparator will reduce the overall power dissipation, area & delay thereby increasing the efficiency of ALU.

X.   DESIGN OF ALU WITH GDI COMPARATOR EXISTING TECHNOLOGIES

Arithmetic unit in ALU consists of adder & subtractor and logic unit consists of logic gates such as inverter, AND, NAND, OR, NOR, XOR, XNOR. So design of ALU includes design of sub modules of arithmetic & logic unit.

Fig.19. ALU block diagram

A) Cmos ALU With GDI Comparator Design

Fig.20. Schematic of CMOS ALU with GDI comparator

B) Transmission gate ALU with GDI comparator design
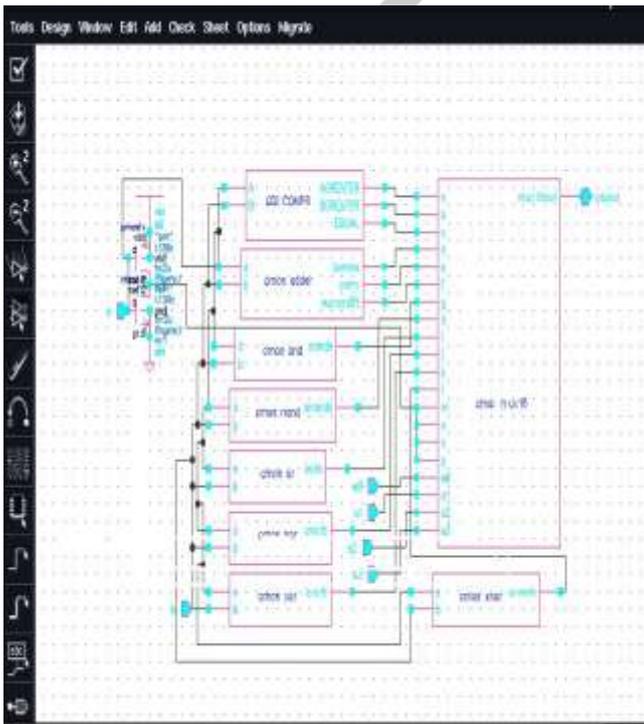

Fig.21. Schematic of TG ALU with GDI comparator

C) Pass transistor ALU With GDI Comparator Design

Fig.22. Schematic of PT ALU with GDI comparator

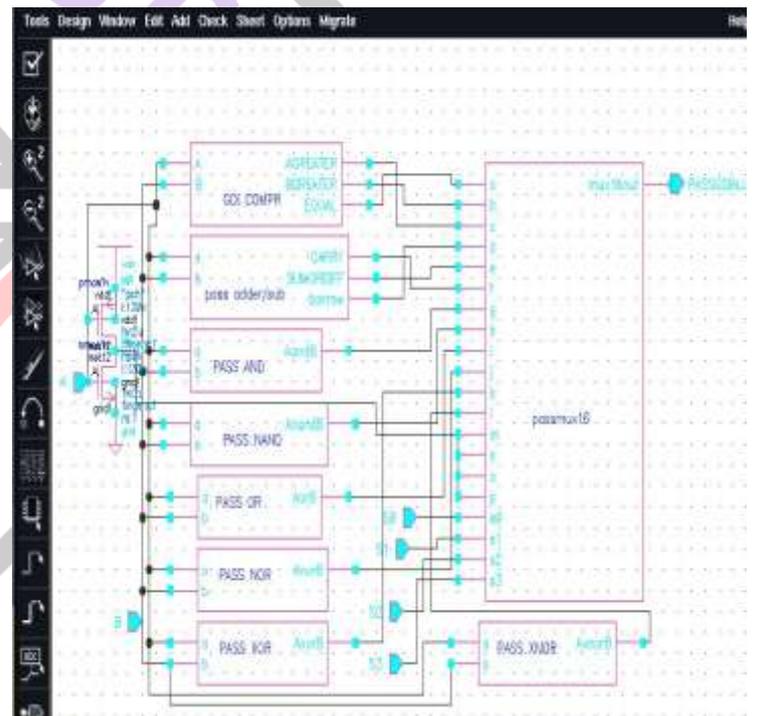D) *Comparison Of Existing ALU's With Existing ALU Designed Using GDI Comparator*

Table.V

Comparison Of Existing ALU's With Existing ALU Designed Using GDI Comparator

ALU TECHNOLOGY	AVERAGE POWER DISSIPATION(W)	DELAY(ns)	POWER*DELAY PRODUCT(w*ns)
CMOS ALU	0.0810	0.1501	0.0121
CMOS ALU WITH GDI COMPARATOR	0.0771	0.1502	0.0115
TG ALU	0.06047	0.1333	0.008
TG ALU WITH GDI COMPARATOR	0.0570	0.1331	0.0075
PT ALU	0.0528	0.09269	0.0048
PT ALU WITH GDI COMPARATOR	0.04722	0.09263	0.0043

From the comparison it is clear that ALU that uses GDI comparator have low power dissipation. Eventhough delay slightly increases, power delay is found to be less in case of ALU with GDI comparator.

So as it is observed that GDI technology reduces the overall power dissipation & power delay product of comparator and such comparator shows better performance in ALU, all blocks of ALU can be designed using GDI technique inorder to achieve a good performance ALU.

XI. DESIGN OF ALU USING PROPOSED GDI & MOD-GDI TECHNOLOGY
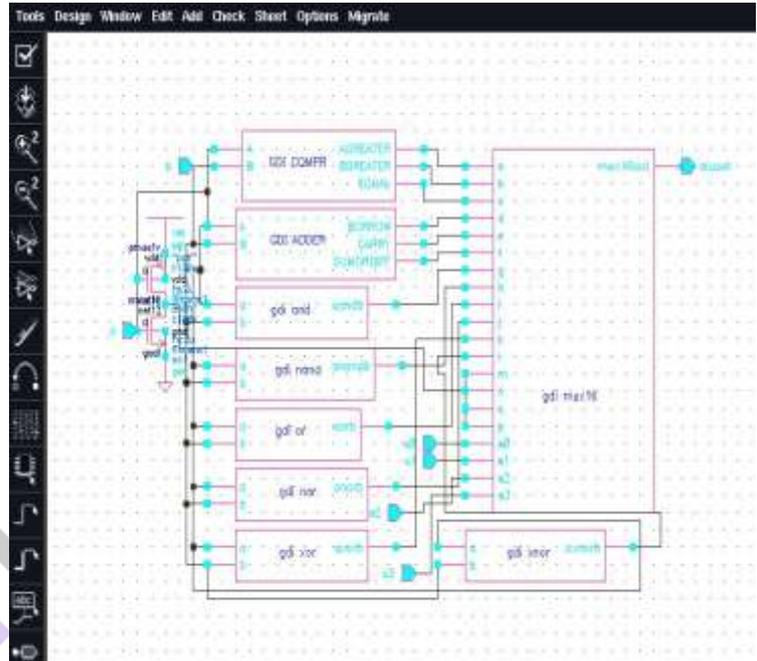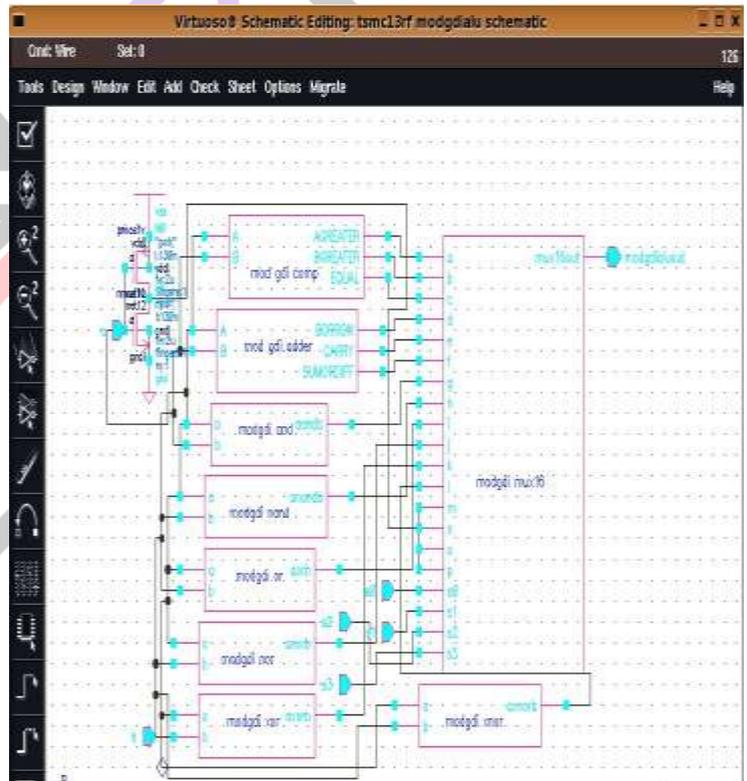
A) *GDI ALU Design*

Fig.23. Schematic of GDI ALU

B) *MOD-GDI ALU Design*

XII. COMPARISON OF EXISTING ALU'S WITH GDI & MOD-GDI ALU

Table.V

Comparison Of Existing ALU's With GDI & MOD-GDI ALU

ALU TECHNOLOGY	AVERAGE POWER DISSIPATION(W)	DELAY(ns)	POWER*DELAY PRODUCT(w*ns)
CMOS ALU	0.0810	0.1501	0.0121
TG ALU	0.06047	0.1333	0.008
PT ALU	0.0528	0.09269	0.0048
GDI ALU	0.0292	0.0954	0.0027
MOD-GDI ALU	0.0600	0.0668	0.0040

From the overall simulation results & analysis, GDI technology is found to be low power dissipation & power delay product. But it suffers from swing degradation. To overcome that issue mod- gdi technique was introduced. MOD-GDI ALU is found to be low delay & power delay product & more efficient as compared to other technologies.

XIII. CONCLUSION

GDI Comparator has shown good performance in terms of power delay product compared to CMOS, Transmission gates & pass transistor design technologies. Low power dissipation & area of the proposed GDI comparator results into an optimized area & power consumption in the design of ALU. From the analysis that GDI comparator reduces overall power consumption and area of ALU, all blocks of ALU are designed using GDI technology It is found that there is a noticeable reduction in power delay product of ALU compared to other technologies. Swing degradation affects GDI technology but it can be overcome using modified GDI logic style Hence, this new design is good option for low power & area efficient system design

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Author's profile:

Author-1:

Mr. KIRAN BALU K received his BTech degree in Electronics and Communication Engineering from Al- Ameen engineering college in 2013 and pursuing MTech in VLSI And Embedded system in Mangalam College Of Engineering,. He is interested in the area of VLSI.

Author-2:

Ms. BINU MANOHAR,Assistant Professor, Department of ECE, Mangalam college of engineering, Ettumanoor, Kottayam. She has completed M.Tech VLSI Design in Amritha school of engineering, Coimbature.