Implementation of an efficient full adder Using Systematic Cell Design Methodology

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***Abstract*— In this paper, an efficient full adder using Systematic Cell Design Methodology (SCDM) is explained. The design is first implemented for 1 bit and then extended to 4 bit also. The circuit was implemented using Mentor Graphics tools at 180 nm technology. Performance parameters like average power, average propagation delay and Power Delay Product (PDP) are compared with existing hybrid adders like FADPL and FASRCPL. The proposed adder has less number of transistors in the critical path leading to less propagation delay. The use of transmission gate throughout the design ensures high driving capability and full voltage swing at the output. The proposed adder is found to be working efficiently when compared to other adders in terms of average power, average propagation delay and PDP.**

***IndexTerms*—Systematic cell design methodology, three input XOR/XNOR, full adder, transmission gate, low power high performance**

I. INTRODUCTION

The advancement of technology has increased the demand for low power electronic systems. Since these low power systems provide long lasting battery operation, they can be used for portable applications. On the other hand, there is a requirement for high speed designs so that efficient operation at high frequencies could be ensured. Unfortunately, to reduce the power of a circuit one must usually compromise on its speed, since lower power translates into smaller current which would ultimately lead to a slower circuit. As a result a useful metric used in such cases is the Power Delay Product (PDP) which can be used to characterize the overall performance of a system. The Power-Delay Product (PDP) refers to the quantity of energy spent throughout the conclusion of a determined task, and stands as the more truthful performance metric when examining optimizations of a module designed and tested using completely different technologies, operational frequencies, and scenarios [3].In the majority of systems, the adder is an element of the vital path that determines the general performance of the system. It is primarily employed in lot of VLSI systems like microprocessors and application specific DSP design. Additionally to its main task, that is, adding 2 numbers, it is employed in several alternative helpful operations like subtraction, multiplication, address calculation, etc. All these operations are realized by complex system of transistors. The critical path consists of transistors that produce the maximum time-delay in the output signal. The behavior of transistors in the critical path essentially determines the performance of the entire system. Hence the performance of the adders can be considered as extremely significant for VLSI systems.

Many papers have been published so far which compete in designing better circuits [1],[2],[3].Though the circuits depend on creative design ideas, they do not follow a systematic approach. As a result such circuits [3] suffer from certain drawbacks.

1. The logic styles incorporated in such circuits lack complete voltage swing in some internal nodes thereby leading to static power dissipation.
2. Most of the circuits cannot sustain low voltage operation due to output signal degradation.
3. Dynamic power consumption prevails for non-balanced propagation delays, which thereby result to glitches at the output.

The above mentioned drawbacks could be solved by following a well organized design methodology. Cell Design Methodology has been introduced [4],[5] which is used to design limited functions. This Cell Design Methodology is later improved to a Systematic Cell Design Methodology (SCDM) for the design of a three input XOR/XNOR structure [6]. The methodology systematically generates Elementary Basic Cell (EBC) using Binary Decision Diagram (BDD) and wisely chooses the circuit components based on a specific target [6].The resultant XOR/XNOR structure was found to have full swing and fairly balanced output.

This paper proposes a full adder designed using systematic cell design methodology. A carry/carry-inverse block is designed in addition to the three input XOR/XNOR structure to form the final full adder. The whole design is done using transmission gates which provide full output voltage swing, increase circuit driving capability and eliminate the need for optimization techniques. The resultant adder is compared with already existing hybrid adders like FA_DPL (Dual Pass-transistor Logic) and FA_SRCPL (Swing Restored Complimentary Pass Transistor Logic)[3].The proposed adder is symmetric and is comparatively PDP efficient. A four bit structure of the proposed adder is developed to analyze its performance in real environment. The entire circuit is drawn using Mentor Graphics Pyxis tool and simulated using Eldo simulator.

II. THREE INPUT XOR/XNOR USING SYSTEMATIC CELL DESIGN METHODOLOGY

The SCDM aims in attaining the target by following a sequence of steps in a systematic way. The target considered is Power-Delay Product (PDP). The main design goals of SCDM are generating balanced outputs, symmetric and power-ground free structure and less number of transistors in the critical path [6].The methodology mainly involves Elementary Basic Cell (EBC) generation and wise selection of mechanisms and cells. The EBC follows a sequence of steps.

1) Representation of Binary Decision Tree (BDT) of three input XOR/XNOR structure.
2) Application of reduction rules
3) Substitution of $\overline{Y}$ for 0 and Y for 1
4) Disjointing simplified symbol

The BDT of three input XOR/XNOR is initially represented using seven 2x1 MUX blocks were A, B and C are the select lines which control the inputs at each corresponding level. A_1,A_2,A_3,A_4,B_1,B_2 and C_1 are the outputs of the respective MUX blocks as shown in Fig.1(a). The inputs and outputs of each block is shown in the Table 1. The BDT is then simplified by the application of reduction rules as shown in Fig.1(b) which include elimination, merging and coupling rules. The coupling rule aim in obtaining all possible equivalent trees by interchanging the order of controls. Then the inputs '1' and '0' are replaced by Y and $\overline{Y}$ respectively. At last each block is disjointed into individual units as shown in Fig.1(c), the plus sign with x input control and the negative sign with $\bar{x}$ input control. The EBC thus extracted shown in Fig.1 (d) has eight elements leading to two outputs. The pins of the central section (In1-In4 and G1-G4) refer to A or B, or their complements while that of external section G5-G8 refer to C or its compliment. The 3 input XOR/XNOR structure shown in Fig.1 (e) is finally obtained by replacing the elements with transmission gates and the control inputs with respective input signals.

Table 1

Select lines			Outputs of each MUX block						
A	B	C	A_1	A_2	A_3	A_4	B_1	B_2	C_1
0	0	0	0	1	1	0	0	1	0
0	0	1	0	1	1	0	0	1	1
0	1	0	0	1	1	0	1	0	1
0	1	1	0	1	1	0	1	0	0
1	0	0	1	0	0	1	1	0	1
1	0	1	1	0	0	1	1	0	0
1	1	0	1	0	0	1	0	1	0
1	1	1	1	0	0	1	0	1	1

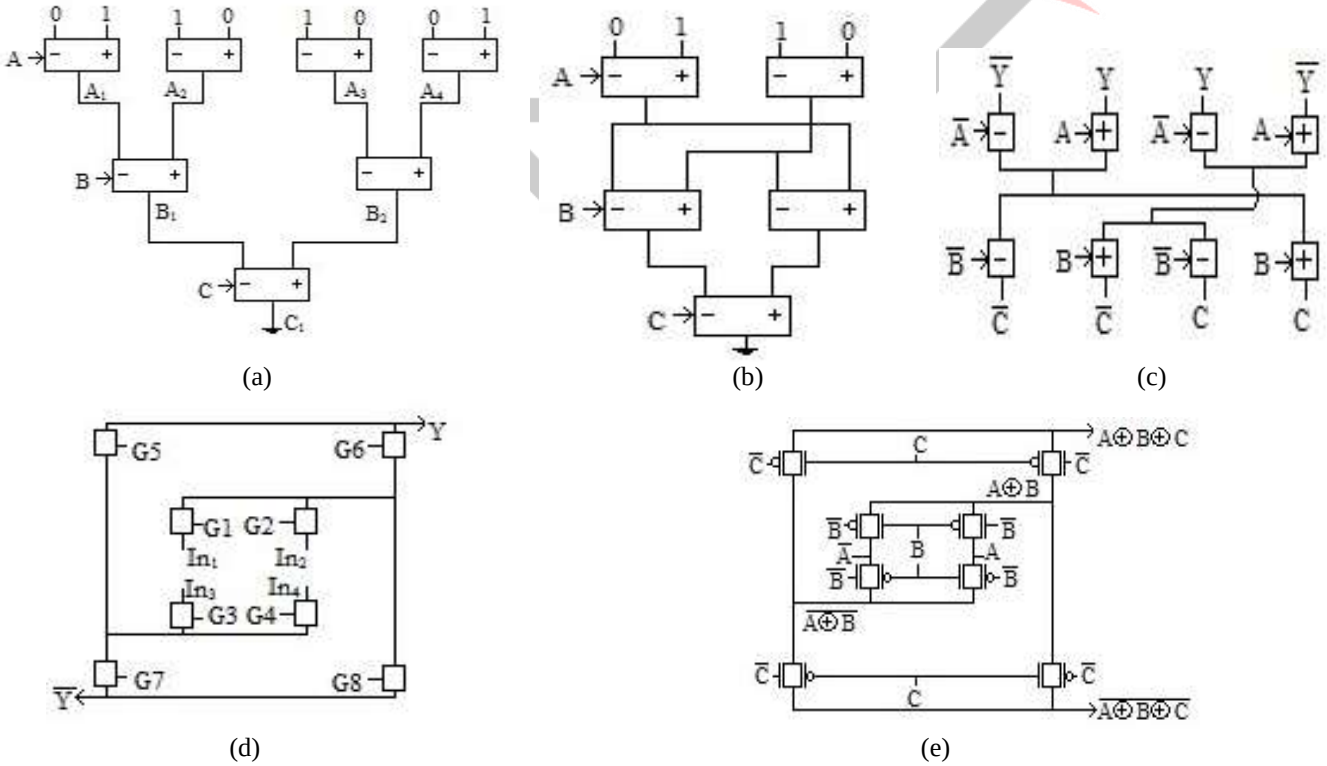

Fig.1 (a) BDT representation of 3 input XOR/XNOR. (b) Applying reduction rules.(c)Substitution and disjointing. (d) EBC. (e) 3 input XOR/XNOR structure.

III. PROPOSED FULL ADDER DESIGN

The three input XOR/XNOR structure is extended to a full adder by the addition of carry/carry-inverse block. The carry/carry-inverse block design is deducted by analyzing the truth table of a full adder. If the inputs A and B are equal, Carry=B, $\overline{\text{Carry}} = \overline{\text{B}}$; else input Carry=C, $\overline{\text{Carry}} = \overline{\text{C}}$.

$$\text{Carry} = \text{B}(\text{A} \odot \text{B}) + \text{C}(\text{A} \oplus \text{B}) \ldots (1)$$

$$\overline{\text{Carry}} = \overline{\text{B}}(\text{A} \odot \text{B}) + \overline{\text{C}}(\text{A} \oplus \text{B}) \ldots (2)$$

The whole design is done using transmission gates which provide full voltage swing at the output. The resulting circuit is symmetric, power-ground free and possesses balanced outputs. The proposed full adder structure is shown in Fig.2.

IV. SIMULATION RESULTS

The proposed adder is set up using Mentor Graphics Pyxis tool and the simulation is done using Mentor Graphics ELDO tool based on TSMC 0.18-µm technology. The propagation delay is measured between C, Carry and $\overline{\text{C}}$, $\overline{\text{Carry}}$ respectively keeping inputs A and B constant. The average propagation delay thus obtained is 23ps and the average power dissipation is 475.153pW. The proposed adder is then compared with two existing hybrid adders, FA_SRCPL and FA_DPL [3] to evaluate its performance based on average power, average delay and PDP. The proposed adder is found to have less PDP compared to other two adders. The corresponding results are shown in Table 2.

In real time conditions a single bit adder may not work properly since the inputs are not fed directly. Instead they are fed by the outputs of the preceding stages. To analyze the success of the proposed adder during its actual use in VLSI applications, a simulation test bench is set up as shown in Fig.3. To create a realistic environment, inverters are added at the input and output of the test bench. The inverters at the input add the effect of input capacitance while that at the output ensure proper loading conditions. The test bench is applied to the proposed adder, FA_SRCPL and FA_DPL. The results of the adders using simulation test bench is shown in Table 3. It is observed that the proposed adder is comparatively efficient with respect to average power, average delay and PDP.

V. PERFORMANCE OF 4 BIT ADDER

A 4 bit ripple carry adder [Fig.4] is implemented as an extension to the proposed 1 bit full adder. The carry propagates all the way to the last adder in the ripple carry adder structure. The performance evaluation is carried out using 180 nm technology. The 4 bit structure of the proposed adder is compared with four bit CMOS adder. It is observed [Table 4] that the four bit structure of proposed adder is efficient compared to the four bit CMOS adder with respect to average power, average carry propagation delay and PDP.

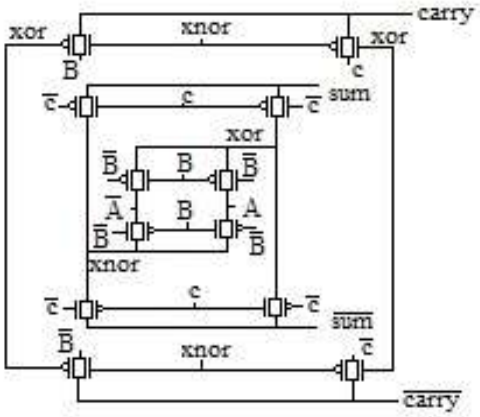

Fig.2.Circuit diagram of proposed full adder

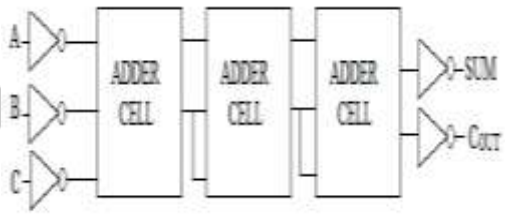

Fig.3.Simulation Test Bench

Table 2
Simulation results in 180 nm technology
(Power in picoWatt, Delay in picoSecond And PDP in attoJoule)

Type of adder	Average Power	Average Delay	Power-Delay Product
FA_DPL	1284.200	52.918	0.067
FA_SRCPL	930.200	54.349	0.050
Proposed Adder	475.153	23.00	0.010

Table 3
Simulation Results in 180 nm technology using simulation test bench
(Power in nanoWatt, Delay in picoSecond And PDP in attoJoule)

Type of adder	Average Power	Average Delay	Power-Delay Product
FA_DPL	3.9712	2427.6	9.640
FA_SRCPL	3.0132	1596.7	4.811
Proposed Adder	1.4701	378.364	0.556

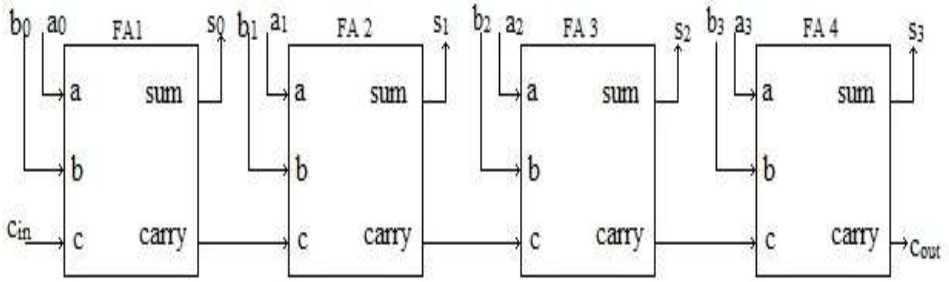

Fig.4. Four bit ripple carry adder using 1 bit proposed adder with true outputs

Table 4
Simulation results of 4 bit adders in 180 nm technology
(Power in nanoWatt, Delay in picoSecond and PDP in attoJoule)

Type of adder	Average Power	Average Propagation Delay	Power-Delay Product
4 bit CMOS adder	3.8072	50.899	0.193
4 bit Proposed Adder	1.4578	53.820	0.078

VI. CONCLUSION

In this paper a 1 bit full adder is proposed using SCDM which is later extended to 4 bit ripple carry adder. The simulation was done using Mentor Graphics Pyxis and Eldo tool with 180 nm technology and compared with existing hybrid adders like FA_DPL and FA_SRCPL. The use of SCDM as the design methodology ensures a symmetric and power-ground free structure. The simulation results prove that the proposed adder offer improved PDP compared to existing hybrid adders.

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