Low power VLSI design techniques- A detailed review

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***Abstract*— Power dissipation has emerged as an important design parameter in the design of VLSI chips, especially in portable computing and personal communication applications. This paper discusses in detail the various low power dissipation techniques used at different levels of abstractions. It also focuses on the recent new techniques developed for lowering the power dissipation in a VLSI chip and adopted widely by the industry.**

***IndexTerms*— Low Power, Abstraction Level.**

Introduction

PDAs with longer battery life are highly in demand. As these digital gadgets are battery powered hence reducing power consumption is indispensable. This can be done by implementing proper power management right from the architecture stage and low power techniques should be apply at various levels of abstractions i.e. from system level to layout level[6]. Moreover limiting the power dissipation is a trade-off between- area, speed and power. This paper discusses the various low power techniques implemented in a VLSI chip design technology, at different level of abstraction. It also covers the recent techniques used in industry for low power dissipation.

Sources of Power Dissipation in a VLSI chip

The three major components of power dissipation in a VLSI or ULSI chip, which are well known, are as follows:

- Dynamic power
- Short-Circuit power
- Leakage power

The percentage of each power dissipation component depends on the application and technology of the chip.

Approximate Contribution of Different Power Dissipation Components in a Chip

(a) Dynamic Power Dissipation – 80% to 90%
   - Clock power contributes to 45-60% of total dynamic power dissipation.

(b) Short Circuit Power Dissipation – 0% to 5%

(c) Leakage Power – 10% to 30%
   - But as technology size shrinks leakage power is a major issue and it reaches nearly 50% of overall power dissipation for 0.07µm technology size.

Power Reduction at Different Levels of Abstraction:

Behavior/Algorithm ---- 90%
Architecture ---------- 11%
Logic ---------- 15%
Circuit ---------- 30%
Physical Design ------- 20%

Low Power Techniques at various abstraction levels

Low Power techniques are applied at different levels of abstraction. Table 1 shows the various low power techniques.

Table 1

Different Levels of Abstraction	Low Power Techniques Used
System Level	System Partitioning, Power Down,Instruction Level Optimization, Hardware-softwareCo-design, Dynamic Power Management, Variable VoltageTechnique
Algorithm Level	Complexity, Concurrency, Regularity
Architecture Level	Parallelism, Pipelining, Clock Gating, Intercommunication and Interconnect Optimization

Logic Level	Path balancing by loweringVdd making delay of all paths equal and Re-sizing, Glitch Reduction.
Circuit Level	Transistor Sizing, Energy Recovery, Library Cell design
Technology Level	Threshold Reduction or Multi-threshold Devices

Following techniques are discussed below briefly which can be used effectively to reduce the power consumption of a VLSI system design cycle.[1][2][3][5][8]

System Level:

- **System Partitioning:**In a VLSI chip many portion of the circuit is inactive during execution of certain task. Hence these inactive portions toggles & consumes power. These useless toggling or switching can be avoided by implementing proper power management techniques and disabling these portions of circuit while they are not doing any useful work. Another approach is partitioning the complete system into different parts such that unnecessary switching activities at a time are localized in one part but this is possible only if the partitioned parts do not depend on each other during their execution. Hence by doing this only one part will be enabled at a time and rest will be disabled which in turn reduces power dissipation.

- **Instruction Level Optimization:** This technique is basically used in processing unit of general purpose microprocessors, DSP and Microcontrollers. In this technique we chose set of those instructions which consumes minimum power for executing application software. Also instruction encoding technique is utilized here for low power instruction fetches.

- **Hardware Software Co-design:** It is defined as the simultaneous design of both hardware and software to implement so as power reduction is achieved. This technique is basically implemented in SoC i.e. System on Chip, microprocessors, DSP Processors, ASIC Cores, memory etc. here the complex designed system is partitioned to perform different tasks right from the early stages of design process so that it may reduce many design problems.

- **Memory Design Technique:** This technique basically focuses on placing memory blocks on chip i.e. supporting cache memory so that power consumption can be reduced.

- **Dynamic Power Management:** In this technique the partitioned system blocks are inactivated by allowing them to enter low power sleep mode. Hence power is saved.

Architecture Level:

- **Parallelism and Pipe-lining:** The key idea behind this technique is to reduce the Power supply (Vdd) level to save power and use parallel-pipeline architecture to balance the performance degradation caused due to reduced power supply level.

- **Block Disabling Technique and Clock Gating:** In block disabling technique, some blocks of the system which are not used during the execution of some particular tasks or clock cycles are inactivated or disabled. This reduces the power consumption. Clock gating is disabling the clock signal to those portions of chip which are inactive during executing a task or instruction. This saves a lot of power as clock network dissipates 40% of overall power dissipation.

- **Interconnect and Intercommunication Optimization:** A significant portion of power in complex CMOSVLSI circuits is dissipated by buses and global communications. Hence techniques like data encoding andlow swing signalling are used for power reduction. Data encoding or compression can have a high impact on power reduction. For example data buses tends to have sequential behaviour instead we can have gray code for optimal switching.

Logic Level:

1) **(a)Path Equalization -Lower Vdd:** Apart from critical path in a system other paths are faster and hence one can lower the supply voltage of these fast paths until their delay becomes similar to critical path.

(b)Path Equalization – Resizing: In this technique the gates along the fast paths are downsized to reduce their input capacitance which in turn reduces the power-consumption. Resizing does not always imply downsizing. Power can also be reduced by increasing the size of heavily loaded gates to increase their output slew rate.

2) **Glitch reduction:** Glitches are unwanted spurious switching activity which appears in circuit due to unequal delay in the paths. Glitches consume 70% of dynamic power dissipation. Above discussed techniques which equalizes the delay in the paths also reduces the glitches.

Circuit Level:

1) **Library Cell Design:** It lies at the heart of circuit level techniques to reduce power-consumption. From the power view point most power consuming cells in design library are: Flip-flops, Latches & Adder cells. These blocks are most used by any CMOS circuit. Also flip-flops and latches are clock driven memory element so using low power design of these blocks reduces clock power consumption too.

3) **Transistor Sizing:** It is similar to gate sizing but with the difference that in transistor sizing any one transistor can be sized independently as compared to gate sizing where all the transistors are sized together. Hence transistor sizing is done to reduce delay and area in a VLSI chip. The critical path transistor can be sized to obtain better power and delay performance.

Technology Level:

1. **MTCMOS:** Various MOS characteristics are supervised by the threshold voltage of the cell. Sub-threshold current is the current between source and drain when the gate voltage is below threshold voltage. Mathematical expression shown in equation (1), for approximate value of this sub-threshold current is :

$$I_{SUB} = I_o . e^{\frac{V_{gs} - V_{th}}{\eta V_T}} [1 - e^{\frac{V_{DS}}{V_T}}] \quad (1)$$

From above equation we can see that sub-threshold current decreases as V_T increases. So higher V_T transistors are placed to decrease this current. In this technique multiple threshold CMOS transistors are used. Transistors with low threshold voltage are placed at critical path while transistors with high threshold value are placed at non critical path. Main aim of such circuit is to maximize the performance & reduce the leakage but done with trading off delay reduction by placing low threshold transistors causing faster gate transitions.

Advanced Low Power Techniques:

1. **Multi V_{DD} Technique(Static Voltage Scaling):** From equation (2),

$$P_{DYNAMIC} = (C. V_{DD}^2 . f_{clk})/2 \quad (2)$$

We know that, there is a quadratic relationship between device voltage V_{DD} and dynamic power consumption. Hence to reduce the dynamic voltage substantially one has to reduce the supply voltage. However, voltage reduction has its downside as well. Propagation delay of a cell is given by the equation (3) given below:

$$T_D = C . V_{DD} / k. (V_{DD} - V_T)^2 \quad (3)$$

Here we can say that as V_{DD} decreases delay increases which in turn decreases the frequency of operation. Hence solution to this problem is to create voltage islands in the design where low performance & slow peripherals can be powered up by lower supply voltage and high performance blocks can be powered up by higher supply voltage. But while designing such voltage island one has to use appropriate voltage level shifters across the signals which talk across the voltage domains.

2. **Dynamic Voltage & frequency scaling:** Static voltage scaling technique is not adaptive to the application needs and voltage supply to a block cannot be changed once designed. So to overcome such limitations Dynamic Voltage Scaling technique is used. In this technique a regulator is used, which can be programmed to deliver voltage levels as required by different blocks of the chip. Hence, various blocks can get configurable voltage and the customer/user can change the voltage settings as per the application settings. This also saves dynamic power. Also this voltage scaling block can be clubbed with dynamic frequency scaling where the frequency of a block can be changed by the software as needed. Therefore, a block running on lower V_{DD} can be clocked by a slower clock while maintaining the performance and functional requirements. This technique helps reduce dynamic as well as leakage power consumption in the device.

3. **Gate Diffusion Input (GDI):** GDI is an efficient alternative for Conventional CMOS design in terms of area and power dissipation. The GDI technique has less area and less power dissipation compared to the CMOS design. A basic GDI cell as shown in fig. 1 consists of four terminals- G (common gate input to both pMOS and nMOS transistors), P (outer diffusion node of pMOS), N (outer diffusion node of nMOS transistor), D (common diffusion of both transistors). P, D and N . It is implemented using twin-well CMOS or Silicon on Insulator (SOI) technologies. Leakage components like GIDL, reverse bias currents can be controlled very effectively using SOI technique. By using GDI technique, it is possible to reduce the transistor count, power dissipation, propagation delay also.

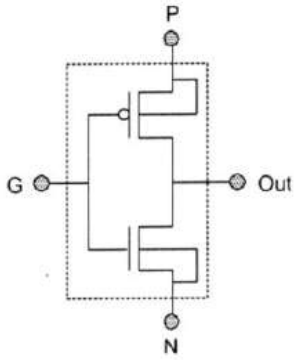

Figure 1: Basic GDI Cell

4. **Well Biasing Technique:** With multi-threshold transistors, in principle, we can solve the quiescent or static leakage problem, but they require additional circuits that modulate substrate voltage in stand-by. Fast and accurate body-bias control with control circuit is quite challenging, and requires carefully designed closed-loop control. When the circuit is in standby mode the bulk/body of both PMOS and NMOS are biased by third supply voltage to increase the V_T of the MOSFET as shown in the Figure. However during normal operation they are switched back to reduce the V_T.

5. **Adiabatic Logic:** Adiabatic logic[4] is based on charge recovery principle. It reuses the energy which is dissipated during the charging and discharging process of circuit operation. As the name itself indicates that instead of dissipating the stored energy during charging process at the output node towards ground it recycles the energy back to the power supply thereby reducing the overall power dissipation and hence the power consumption also decreases. The adiabatic logic uses AC power supply instead of constant DC supply, this is one of the main reasons in the reduction of power dissipation.

Conclusion: In this paper various low power dissipation techniques have been discussed in detail, at different levels of abstraction. We conclude that implementing these techniques right from behavior/algorithm level reduces the power dissipation. Also the recent techniques of power dissipation used presently are discussed. Reduction in power dissipation at various abstraction levels is still a topic of immense research by industry & academicians. These methods are implemented with state of the art EDA tools.

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