A Low Power 4X 4 Multiplier Design using (5-T)Half Adder,(8-T)Full Adder &(2-T) AND Gate

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***Abstract*— In this paper, we propose a new technique for implementing a low power high speed multiplier using full adder consisting of minimum no. of transistors (8-T). Multiplier circuits are used comprehensively in Application Specific Integrated Circuits (ASICs). Thus it is desirable to have high speed operation for the sub components. The explored method of implementation achieves a high speed low power design for the multiplier. Simulated results indicate the superior performance of the proposed technique over conventional CMOS multiplier. Detailed comparison of simulated results for the conventional and present method of implementation is presented.**

Keywords— 2-T AND; 8-T Full Adder; 4x4 Multiplier; 2-T MUX; Pass transistor logic; 3-T XOR;

I. INTRODUCTION (*HEADING 1*)

ECENT years have witnessed tremendous advancement of portable electronic devices powered by batteries with intensive computational capabilities. The power requirements of these devices have increased many folds with the increase in complexity of ICs. In order to produce practically viable economic electronic devices, researchers are investigating new techniques to design low power & high speed circuits with small area of implementation. Now-a-days logic circuits are designed using pass transistor logic techniques [1]. Recently many techniques have been proposed with the objective of improving speed and power consumption [2]-[6]. Two of them, simultaneously developed by Hitachi CPL [4] and DPL [5] are the most notables. The Double Pass-Transistor Logic, developed by Hitachi demonstrated a 1.5ns, 32-bit ALU in 0.25µm CMOS technology [5] and 4.4ns, 54X54 bit multiplier [6]. Similarly many works have been done recently to design 4x4 bit multiplier [7]-[9]. The main objective of our work is to implement the low power high speed multiplier & to make a detailed comparative study with conventional CMOS multiplier. Our multiplier uses less number of transistors in comparison to the conventional multiplier, so that the propagation delay time & power consumption get reduced. It also helps in reducing the layout area thereby decreasing the entire size of a module where this multiplier submodule is used. Power consumption is increasingly becoming the bottleneck in the design of ICs in advanced process technologies. We evaluate them from an industrial product development perspective. We also give a brief outlook to proposals on other levels in the design flow and to future work

II. THEORY AND ARCHITECTURE OF THE MULTIPLIER

A combinational multiplier is a superior model showcasing how simple logic functions (gates, half adders and full adders) can be combined to build a much more complex function. Consider the following example (fig. 1) for binary multiplication of two positive 4-bit integer values.

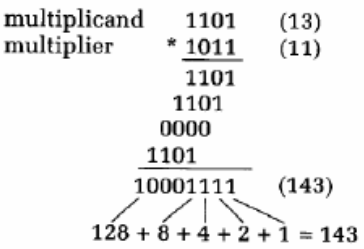


Fig 1: binary multiplication example (4x4)

Here, each bit in the multiplier is multiplied with the multiplicand. Each of the four products is aligned (shifted left) according to the position of the bit in the multiplier that is being multiplied with the multiplicand. The four resulting products are added to form the final result. Therefore for an NxN multiplier, the result is 2N bits wide. With binary numbers, forming the products is much easy. If the multiplier bit is a 1, then the corresponding product is simply an appropriately shifted copy of the multiplicand. If the multiplier bit is a zero, then the product is zero. 1-bit binary multiplication is thus just an AND operation. To build the NxN multiplier let us take an array of a building block consisting of an AND gate and a full adder to get the partial product. The building block is shown in fig. 2 and the 4x4 multiplier in fig. 3 correspondingly. The basic building block consists of an AND gate for computing locally the corresponding partial product (X.Y), an input passed into the block from above (Sum In), and a carry (Cin) passed from a block diagonally above. It generates a carry out bit (COUT) and a new sum out bit (Sum Out). Fig. 3 illustrates the interconnection of these building blocks to construct a 4x4 combinational multiplier.

The Ai values are distributed along block diagonals, and the Bi values are passed along the rows.

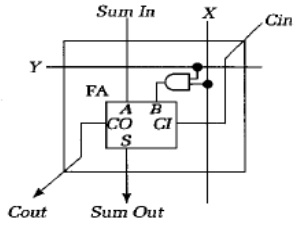


Fig 2. Building block of multiplier

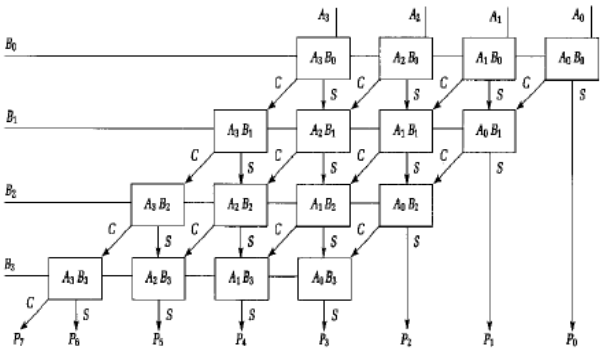


Fig. 3. 4x4 multiplier using 16 nos. of basic building block shown in fig. 2

The modified approach [7] of the above circuit can be made by using sixteen AND gates, six full adders and four nos. of half adders as shown in fig. 4.

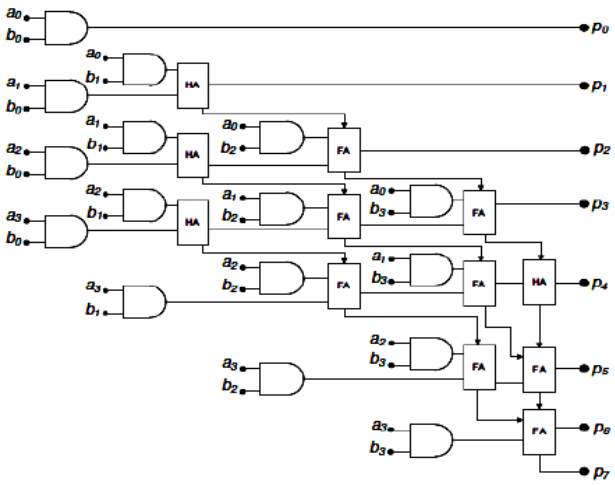


Fig. 4. 4x4 multiplier using AND gate, Half adder and full adder

To design a low power 4x4 multiplier the approach is to design the circuits with minimum nos. of transistors. Here the basic building blocks (half adder, full adder & AND gate) of the 4x4 multiplier shown in fig. 3 and fig. 4 are constructed with minimum no of transistors which are discussed in section III.

III. ARCHITECTURE OF 8-T FA, 2-T AND GATE & 5-T HA

This work presents adder circuits using pass transistor logic based MUX & XOR gate, which contains lesser no. of transistors and achieving better performance. This full adder using pass transistor logic has advantages over CMOS and is characterized by excellent speed and low power. In electronics, Pass-Transistor-Logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic circuits, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages [3]. This reduces the number of active devices, but has the disadvantage that output levels can be no higher than the input level. Each transistor in series has a lower voltage at its output than at its input [10]. For proper operation, design rules define the arrangement of circuits, so that sneak paths, charge sharing, and slow switching can be avoided [11]. Double-Pass-transistor-Logic (DPL) eliminates some of the inverter stages required for Complementary-Pass-transistorLogic (CPL) by using both N and P channel transistors, with dual logic paths for every function [3]. While it has high speed due to low input capacitance, it has only limited capacity to drive a load. Pass transistor logic has become important for the design of low-power high-performance digital circuits due to the smaller node capacitances and reduced transistors count it offers. However, the acceptance and application of this logic depends on the availability of supporting automation tools, e.g. timing simulators, which can accurately analyze the performance of large circuits at a speed, significantly faster than that of SPICE based tools [10].

A. 8-T Full Adder (FA)

A full adder circuit is one of the basic building blocks of a digital design. In general it is made by CMOS technology. In the CMOS technology the full adder is built by 28 transistors. As, the transistor count is quite high the area consumption, leakage power consumption and delay are also high. The decrease in the transistor count reduces the area, Leakage power, delay and noise. The basic circuit of proposed single bit 8-Transistored full adder (8-T FA) is composed of 2 XOR gate to implement the sum out & another two input MUX to implement the carry out. The basic structure of the 2:1 MUX using pass gate transistor logic is shown in fig. 5 [12]. In this configuration we have connected PMOS and NMOS along with a SEL line, as in MUX. As we know that PMOS works on ACTIVE LOW and NMOS works on ACTIVE HIGH. So, when the SEL input is low (0) then the PMOS gets activated, and shows the input IN0 in the output and due to low input (0) the NMOS stands idle, as it is activated in high input. Same for the case, when the SEL input is high (1) then the NMOS gets activated, and shows the input IN1 in the output. Thus this circuitry behaves as a 2:1MUX with SEL line selecting the favorable input for the output.

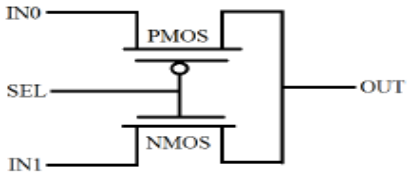


Fig. 5. Basic view of 2T MUX

The second component required to design a full adder with 8 transistors is XOR gate. Conventional XOR gate can be fabricated using Transmission Gate (TG) logic which needs more than 3 transistors. But here is the design of a XOR gate with 3 transistors as shown in fig. 6 below [13],

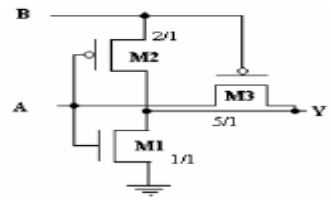


Fig. 6. Basic view of 3T XOR gate

Using 2 input MUX & 2 input XOR gate we can design a 8-T FA as shown in fig. 7 below,

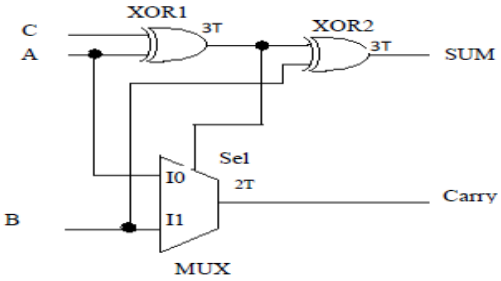


Fig. 7. 8-T FA based on MUX & XOR gates

The digital circuit shown in the fig. 7 can be analyzed logically with the help of simple Boolean algebra. The inputs to XOR 1 gate are A & C. So the output is $A \oplus C$. This output is again XORed with B so the output of XOR2 is,

Sum = $A \oplus B \oplus C$ .....eqn. (1)

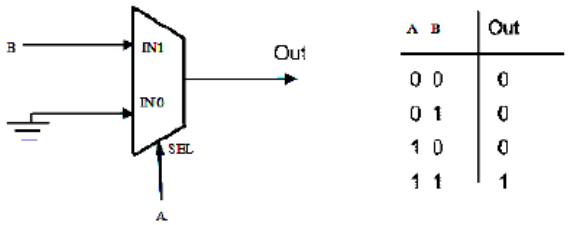
Regarding carry generation the inputs to the MUX are A & B respectively & the select line is $A \oplus C$ So the output becomes,

$$\begin{aligned}
\text{Carry} &= \overline{(A \oplus C)}.A + (A \oplus C).B \\
&= (\overline{A}C + A\overline{C})A + (\overline{A}C + A\overline{C})B \\
&= AC + AB\overline{C} + \overline{A}BC \\
&= AC(B+\overline{B}) + AB\overline{C} + \overline{A}BC \\
&= ABC + A\overline{B}C + AB\overline{C} + \overline{A}BC \\
&= ABC + ABC + ABC + AB\overline{C} + A\overline{B}C + \overline{A}BC \\
&= ABC + AB\overline{C} + ABC + \overline{A}BC + ABC + A\overline{B}C \\
&= AB(C+\overline{C}) + BC(A+\overline{A}) + AC(B+\overline{B}) \\
&= AB + BC + CA
\end{aligned}$$

.....eqn.2

B. 2-T AND Gate

The next module is AND gate which can be easily implemented by the 2-T MUX as shown below in fig. 8,



A	B	Out
0	0	0
0	1	0
1	0	0
1	1	1

Fig. 8. 2-T AND using 2-T MUX

When 'A' value is '0' i.e. 'sel' line is low then IN0 will be selected to the output and as IN0 is grounded so output is always remaining at low state. On the other side when 'A' is '1' i.e. 'sel' line is high IN1 is selected and as 'B' is connected with IN1 so according to the logic level of 'B' output will be either at low or high state following the truth table of AND gate as shown in fig. 8.

C. 5-T Half Adder (HA)

As already we have designed 3-T XOR and 2-T AND gate, now one half adder can be easily designed with five nos. of transistors. Fig. 9 shows 5-T half adder block diagram.

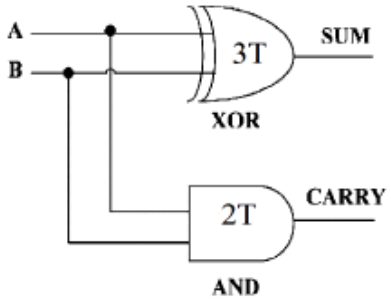


Fig. 9. 5-T HA based 3T XOR & 2T AND

There are three major sources of power dissipation in a digital CMOS circuit: logic transition, short-circuit current and leakage current [5], [6]. The short-circuit current is the direct current passing through the supply and the ground, when both the NMOS and the PMOS transistors are simultaneously active [5], [10]. As the proposed 8-T FA and 5T HA do not havedirect connections to or port (voltage connections to the back gate terminals are not considered), the probability of a direct path formation from positive voltage supply to the ground during switching can be substantially reduced; that is, the power consumption due to short circuit current is considered negligibly small. Furthermore, in the new adder circuits, all of its internal gate nodes are directly excited by the fresh input signals (and), leading to a much faster transition (low rise and fall times) in its output signals. As a result, the power consumption of the following buffer stage can benefit from faster/cleaner Sum and Cout outputs.

IV. SIMULATION

The act of simulating something generally entails on behalf of certain key characteristics or behaviors of a selected physical or abstract system. Simulation can be used to get the functional and timing analysis of the circuit models. Here conventional & our proposed two different 4x4 multiplier circuits are analyzed in standard simulator using 250 nm technology. We implement the conventional multiplier (fig. 3) with basic building block which consists of CMOS full adder using 28-T & CMOS AND gate using 6-T. Thus conventional multiplier has 34-T for each block and 34x16-T for 4x4 stage, where as our proposed multiplier building block has 8-T FA, 2-T AND i.e total 10-T for each block and 10x16-T for 4x4 stage multiplier. The second approach of 4x4 multiplier shown in fig. 4 consists of sixteen AND gates (2T), six full adders (8T) and four nos. of half adders (5T). Therefore it consists of total (16x2)+(6x8)+(4x5) transistors i.e. 90T. The circuits are simulated in schematic editor by providing input combinations as per example 1. The input specifications are tabulated in the table 1 and the results are compared and analyzed.

TABLE 1- INPUT SPECIFICATIONS FOR 250NM TECHNOLOGY SIMULATION

Source Type	Bit
Zero Value	0V
One Value	5V dc
One bit duration	10 ns
Rise time	1 ns
Fall time	1 ns
Bit Parameter (input A)	1101
Bit Parameter (input B)	1011
Stop Time	30 ns

V. SIMULATION RESULTS & ANALYSIS

For testing the proposed multiplier we provide the input combinations as bit parameter of example shown in fig. 1. All the combinations are introduced during the time period between 10ns to 20ns. Thus for the outputs we also concentrate over that particular time period only. We run the simulation over both conventional & proposed two different multipliers architecture. The transient responses of all the circuits are shown below in fig.10, fig. 11 & fig. 12 respectively. After running the simulation the power consumption and delay of the circuits are tested and compared.

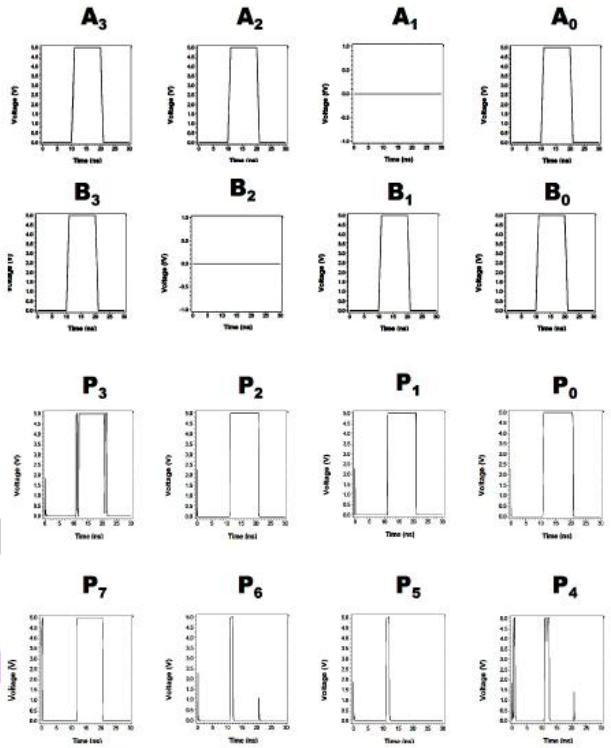


Fig. 10. Transient response of 34x16T Conventional CMOS 4x4 Multiplier A_i: one multiplicand input (4 bits), B_i: one multiplier input (4 bits), P_i: partial product

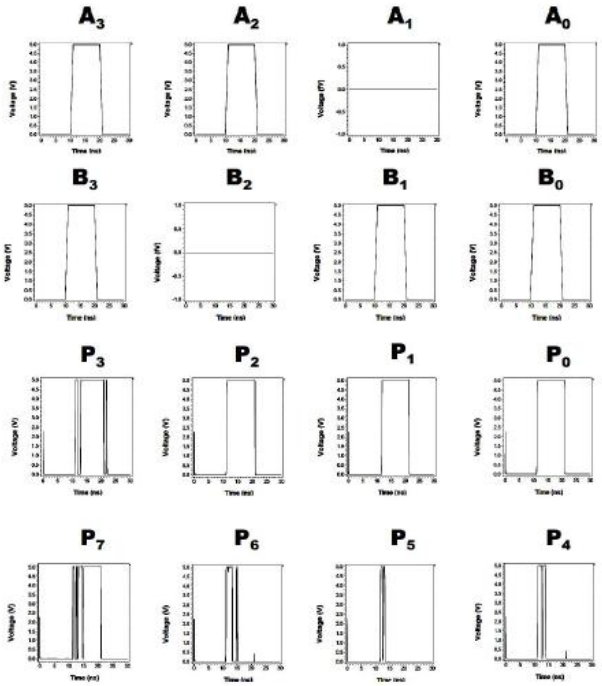


Fig. 11. Transient response of 10x16T Proposed 4x4 Multiplier A_i: one multiplicand input (4 bits), B_i: one multiplier input (4 bits), P_i: partial product

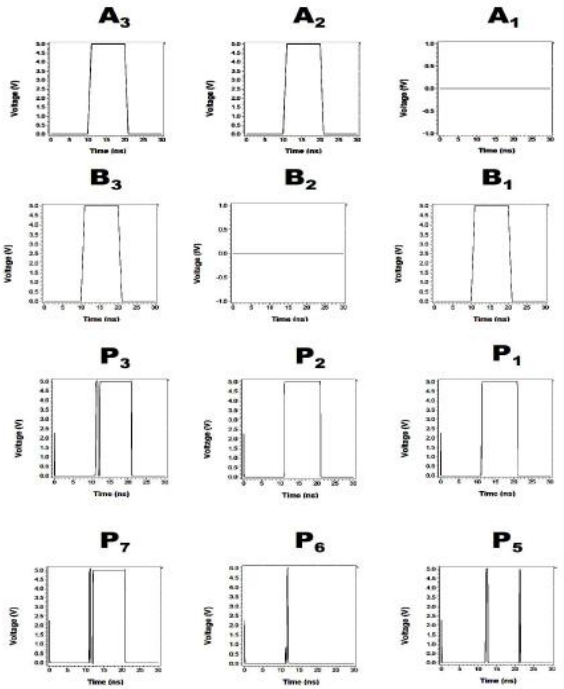


Fig. 12 Transient response of 90-T Proposed 4x4 Multiplier A_i: one multiplicand input (4 bits), B_i: one multiplier input (4 bits), P_i: partial product

From the simulation results (fig. 10, fig. 11 & fig. 12), it can be easily understood that the proposed multipliers have the same functional response as like the conventional multiplier. The power & timing behavior is tabulated in the table 2 below, Regarding area consideration it can be easily understood that with lesser no. of transistor count compared with conventional circuit proposed 90-T and 10x16-T 4x4 multiplier core will be of much lower size compared to 34x16-T CMOS 4x4 multiplier.

TABLE 2: COMPARISN BETWEEN CONVENTIONAL & PROPOSED MULTIPLIER

		34X16T CONVENTIONAL 4X4 MULTIPLIER	10X16T PROPOSED 4X4 MULTIPLIER	90- T PROPOSED 4X4 MULTIPLIER
Power Analysis	*Avg. Power*	56.94557mw	38.78079mw	18.15621mw
	Max Power	.2719556w	.1323385w	.2267146 w
	Min Power	13.85926mw	.8022015mw	.6970550 mw
Transient Delay Analysis	*Rise time delay*	1.9953ns	1.4085ns	1.3875 ns
	Fall time delay:	1.34 ns	1.18 ns	1.2046 ns

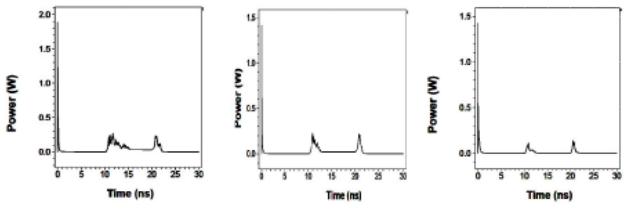


Fig. 13. Power consumption of (a) conventional CMOS multiplier; (b) proposed 10x16 transistor multiplier and (c) proposed 90-T multiplier

conclusion

From the above results it can be concluded that our proposed multiplier has got better performance in terms of speed, power and area consideration in comparison with the conventional CMOS multiplier. It turns out that in contrast to older process technologies, this approach is more suitable for industrial usage in advanced process technologies.

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