IMPLEMENTATION OF MODIFIED DUAL-LOOP PHASE-LOCKED LOOP

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***Abstract*—This paper introduces an enhanced Dual-Loop Phase-Locked Loop (DL-PLL) architecture that combines a Modified design of three Stage Current Starved Voltage-Controlled Oscillator (CSVCO) having an active oscillation range between 6 to 21GHz, with a Frequency Detector (FD) and Phase Detector (PD) loops to achieve superior frequency stability, reduced phase noise, and optimized locking behavior. The dual-loop structure consists of a fast-locking inner loop FD and a low noise outer loop PD, addressing the need for efficient frequency acquisition alongside enhanced steady-state accuracy. The modified three stage CSVCO have wide tuning range, current-starved method brings accurate control over frequency of oscillation. The inclusion of a FD loop improves the frequency comparison and eliminating dead-zone issues, along with the inclusion of a PD loop performs phase detection and reduces the phase noise and jitter in the PLL output. The simulation results shows that DL-PLL having a faster lock times, lower phase noise, and reduced power consumption. This design is suitable for high performance applications, like clock synchronization, communication systems, clock generation in digital circuits, and high-frequency signal synthesis.**

***Index Terms*— Three stage Current Starved Voltage controlled Oscillator (CSVCO), Phase Frequency Detector (PFD), Frequency Detector (FD), Phase Detector (PD), Frequency response, Jitter reduction, Phase Noise**

I. INTRODUCTION

In advanced signal processing systems and communication systems, the Phase-Locked Loops (PLLs) is an important element in frequency synthesis, clock generation, and signal synchronization. The increased requirement of PLL for higher data rates, reduced jitter, lower phase noise and low power consumption remains. Thus the design of efficient PLL architectures has becomes more important. This paper presents a DL-PLL designed in 45nm technology with Cadence virtuoso simulation tool. This includes a design of Modified Three-Stage CSVCO, Frequency Detector (FD), Phase Detector (PD), Loop Filter (LF), and Divide-by-N Network, along with a Feedback, and Quadrature Delayed Feedback. The designed dual-loop structure combines fast-locking inner loop FD for frequency comparison and low-noise outer loop PD for phase comparison to improve both frequency acquirement and steady-state jitter performance. The modified three-stage CSVCO employing current-starved techniques offer enhanced voltage-to-frequency linearity, wider tuning range, and considerably reduced phase noise. By leveraging a FD, the PLL structure excludes dead-zone effects and improves faster frequency comparison, while the adding a PD loop improves total stability and reduces jitter in the output signal. Also, the feedback and Quadrature Delayed Feedback signals are combined to lessen timing errors and enhance the overall phase locking behavior. The feedback system that ensures the PLL can quickly lock to the preferred frequency while sustaining negligible phase error throughout its operation. Through simulation and analysis, this design exhibits greater performance in terms of phase noise reduction, faster locking times, and lower jitter. This work contributes to the growing need for high-performance PLL designs capable of meeting the requirements of future electronic systems.

II. MODIFIED DUAL-LOOP PLL ARCHITECTURE

The DL-PLL shown in Fig.1 separates the tasks of frequency and phase detection, having reduced power consumption, negligible phase noise, and faster locking time with wide acquisition range [1]. The tri-state PFD integrated in a FD circuit with a Voltage-to-Current Converter (VIC) and a frequency detection switch control voltage, and a Phase Detection PD merged VIC for phase detection. This design overcomes the speed limitations of the traditional tri-state PFD based single loop PLL. Key differences in this design lie in the topology of the FD. A XOR based tri-state PFD [3] is used to correct frequency errors and automatically disables the VIC by FD switch when the frequency is locked. The two detection loops are combined using a second-order low-pass filter (LPF), which suppresses voltage ripple on the control side of the voltage-controlled oscillator (VCO). All LPF components are integrated with 45nm technology. The output current from the PD is injected into the LPF, enabling fast phase locking. The FD generates the polarity of the frequency error (indicating whether the VCO frequency is greater or less than the locking frequency), and the VIC FD current is injected into the capacitor (CL) for voltage integration, reducing the frequency error during frequency locking.

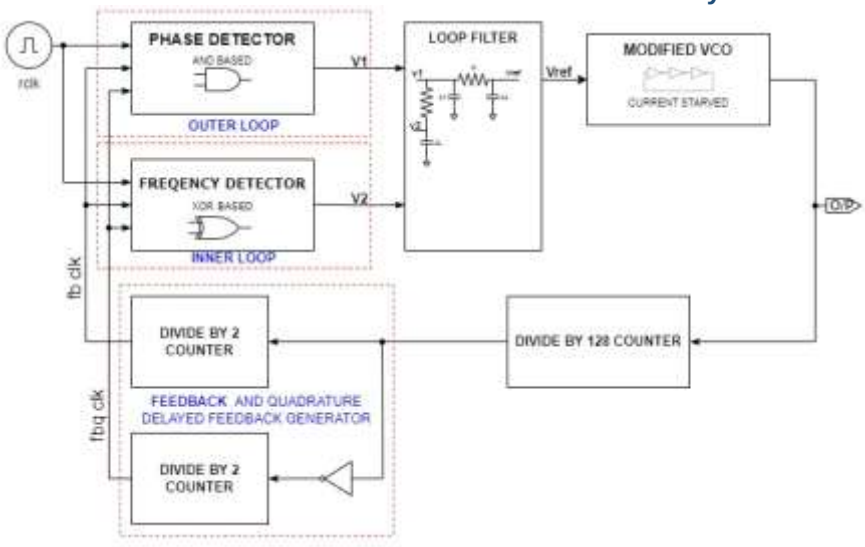

Fig.1 Modified Dual-Loop Phase-Locked Loop Block Diagram

In our dual-loop PLL design, the loop parameters are first optimized based on the phase-detection loop. The locking time may increase due to the settling process dominated by the VCO and the feedback frequency divider network. By carefully setting a small current ratio between the FD and PD, we can eliminate instability risks. This design effectively reduces the overall PLL power consumption while improving jitter performance.

III. PHASE DETECTOR WITH VIC (OUTER LOOP)

Our AND based PD have reduced power consumption by four times compared with the current mode logic based XOR gate PD that consumes more static power [1]. The fig.2 illustrates the diagram of the implemented PD for leading and lagging conditions. The overlapping area between quadrature delayed feedback (Fbq clk) and reference clock (ref clk) for generating IDN is 0 into the loop filter input V1 and minimize the phase error. While the VCO is lagging, the falling edge of feedback clock (Fb clk) lags behind reference clock (ref clk), result in transistor P4 in on state more than that of transistor N5 and gives a charging current to Capacitor C_L to increase the CSVCO frequency. Likewise the VCO leads the falling edge of feedback clock leads reference clock, the overlapping area of quadrature delayed feedback and reference clock for generating I_{DN} discharges Capacitance C_L, decrease the CSVCO frequency for phase locking.

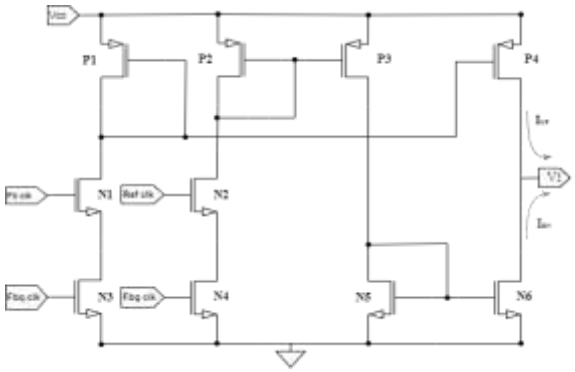

Fig.2 **.AND** Based Phase Detector with VIC

IV. FREQUENCY DETECTOR (INNER LOOP)

A D flip-flop is used to detect frequency error which produces a V_{FD} signal to control the output of VIC_{FD} shown in Fig.3 the quadrature delayed feedback having 90° delay given as D input and the reference clock is given as clock signal while positive edge of Ref Clock the Fbq clk will remains at zero if the phase difference of feedback clock lies between ± 90° with reference clock more than that phase delay considered as frequency shift and the FD output V2 will respond

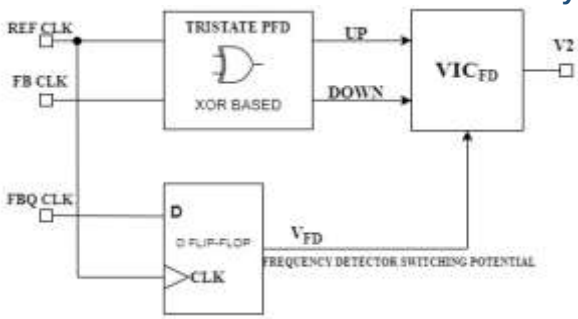

Fig.3. Frequency Detector – Block diagram

V. IMPLEMENTED PFD

Phase Frequency Detector Fig.4 is primarily in pre-charge phase (both reference and feedback clock at logic 0) P2 and P3 drive the node'1 potential to logic high. During evaluation phase, reference clock and feedback clock are compared and UP or DOWN signal is produced (Logic high at 'UP' output when feedback clock lags behind reference clock and logic high at 'DOWN' output when feedback clock leads the reference clock). At idle phase, when both input signals are at logic high UP and DOWN output signals are in logic low or at ground potential.

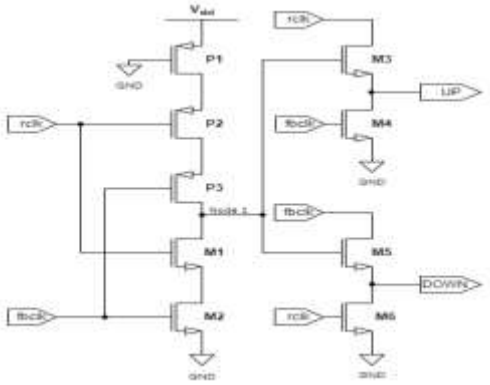

Fig.4 Phase Frequency Detector (XOR Based)

VI. VIC WITH FD SWITCH CONTROLL

Figure.5 shows that if V_{FD} is logic 1or high above threshold the V2 will be present according to leading or lagging feedback frequency else V2 will be in high impedance state

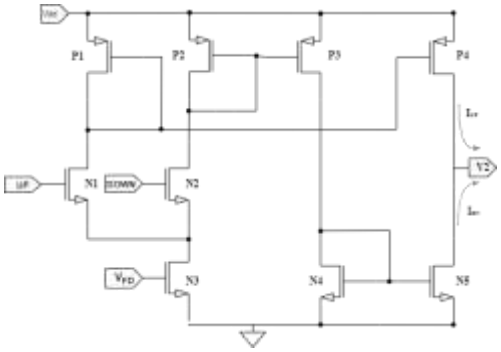

Fig.5 Voltage to Current Converter with FD Switch

VII. LOOP FILTER

Fig.6 A loop filter with a charging capacitor C_L. For a step input signal, the output voltage V_{REF}, which is also the voltage across the capacitor C_L, rises exponentially toward the final value V with a time constant RC. The output voltage V_{REF} can be expressed as

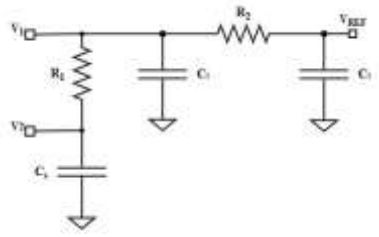

Fig.6 RC filter

$$V_{REF} = V\,(1 - e^{-t/RC}) \qquad (1)$$

Where V_{REF} is the output voltage across the capacitor C_L at time t, V is the final steady-state voltage, Eq.1 R is the resistance, C_L is the capacitance, t is the time elapsed since the input step signal was applied, RC is the time constant of the circuit.

VIII. MODIFIED CURRENT-STARVED VOLTAGE-CONTROLLED OSCILLATOR (CS-VCO):

In Fig.7 CSVCO the output oscillating frequency is determined by the applied input voltage V_{REF}. By varying the V_{REF} the PLL can phase-lock the CSVCO's output oscillating frequency to equal the desired reference signal. The CSVCO is an important component in the PLL system, as its performance directly affects various factors like phase noise, frequency stability, frequency range and overall PLL behaviour.

The number of stages N in the CSVCO circuit can influence its output frequency. The ability to adjust V_{REF} allows for precise control over the VCO's oscillation frequency, making it a key element in maintaining the phase-locked condition in the PLL.

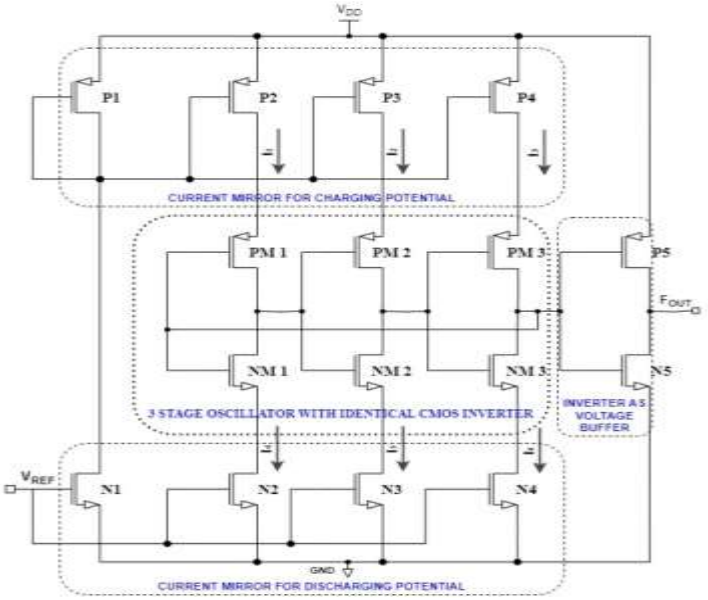

Fig.7. CSVCO

The time it takes to charge and discharge the total capacitance C_{TOTAL} between switching potential V_{SP} to the ground with a constant current source I_{drive} given by the equation

$$t_{rise} = \frac{C_{TOTAL}(V_{DD} - V_{SP})}{I_{drivePMOS}} \qquad (2)$$

$$t_{fall} = \frac{C_{TOTAL} \times V_{SP}}{I_{driveNMOS}} \qquad (3)$$

This Eq.2, Eq.3describes the time required to charge and discharge the total capacitance up to a switching voltage when a constant current is applied. It highlights the relationship between capacitance, voltage, and current in determining the charging time. Vice versa for discharging time

The frequency of oscillation can be derived as - $\boldsymbol{f_{osc} = \frac{1}{N(t_{rise}+t_{fall})} = \frac{I_{DRIVE}}{N.C_{TOTAL}.V_{SP}}}$ (4)

The CMOS Inverter can also call as a floating circuit, because the output of the inverter will be in high impedance state as no input is applied. In this design the three stage ring oscillator does not produce any oscillation at initial conditions, the applied V_{REF}

have initial fluctuating glitches due to the reference clock. This make minimal current fluctuations in ring oscillator inverters that make the output of inverter to change high impedance state to low signal state, it starts oscillating near V_{TH} (threshold voltage) and increase its potential swing up to V_{SP} to Ground voltage rapidly

IX. DIVIDE BY 128 COUNTER

The VCO generates a high-frequency signal, and a feedback divider is used to divide this VCO frequency by a factor N, bringing it closer to the reference frequency. This division allows the PLL to compare the VCO output with the reference frequency to compute the phase error. By adjusting the division factor N, the PLL can lock the system to different frequency ranges. This flexibility allows for the generation of a wide range of frequencies just by changing the divider factor, enabling the PLL to generate accurate output frequencies for various applications such as clock synthesis, frequency modulation, and communication systems. Divide-by-2 counter is one of the simplest types of frequency dividers, often implemented using flip-flops. It takes an input signal and generates an output signal whose frequency is half of the input frequency. This is typically achieved by using a T flip-flop circuit Fig.8 in which the signal undergoes a process of toggling between two states (high and low) with every input positive edge clock cycle [8]. Thus, for every two input clock pulses, the output toggles once, effectively dividing the frequency by two.

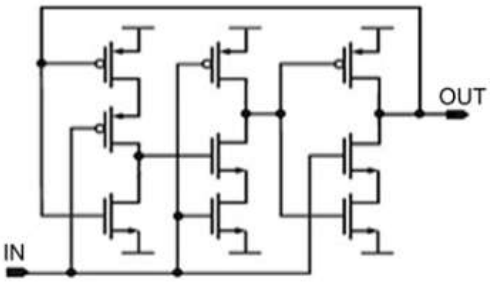

Fig.8 Frequency Divider schematic

The reference clock is multiplied to a ratio of 256 times in this DL- PLL design, here we use divide-by-128 counter and two divide-by-2 counters to get feedback clock and quadrature delayed feedback

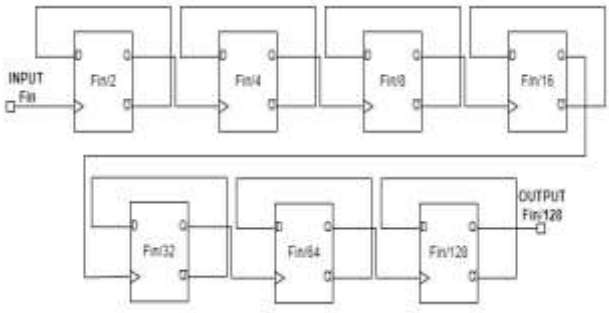

Fig.9 divide by 128 counter block diagram

Seven T flip-flops used to construct divide by 128 counter each T flip-flop performs division of 2 with applied input clock frequency

X. FEEDBACK AND QUADRATURE DELAYED FEEDBACK

In the described scenario, the divide-by-128 counter output is used as the input to two divide-by-2 counters. Fig.10 The input to one of the divide-by-2 counters is passed through an inverter, which results in a 180-degree phase shift. This setup causes the two divide-by-2 counters to produce outputs with a 90-degree phase difference or can be called as quadrature delayed signal

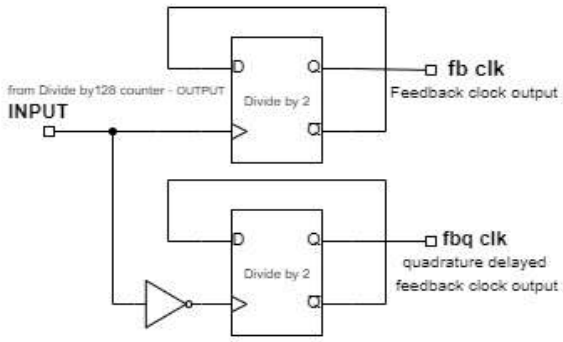

Fig.10 feedback and quadrature delayed feedback generator

XI. PERFORMANCE AND RESULT ANALYSIS

MODIFIED CURRENT STARVED VOLTAGE CONTROLLED OSCILLATOR

Figure.11 Three stage CSVCO implementation in cadence virtuoso modified by adjusting width of transistors to enhance frequency of oscillation range from 6GHz to 21GHz, Fig.12 transient response of modified CSVCO and the transient response analysis results tabulated (Table 1) shows that the oscillation frequency varies from 700mW to 1300mW gradually and get saturates above that given reference potential V_{REF}

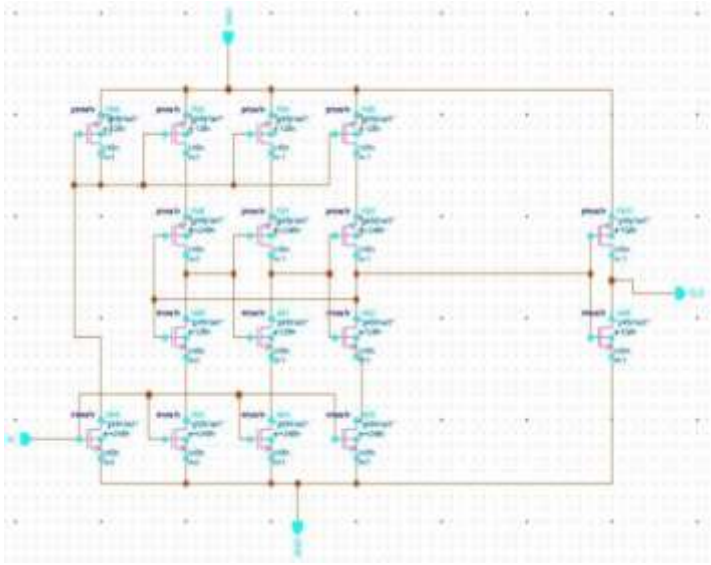

Fig.11 CSVCO Schematic design using cadence virtuoso

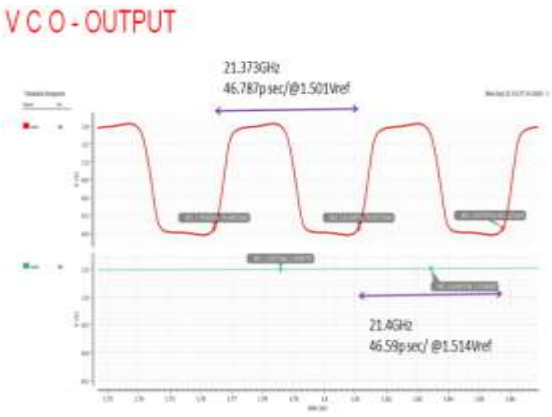

Fig.12. Transient Response of VCO

TABLE 1 CSVCO ANALYSIS

Sl. No.	I/P Voltage(mV)	O/P frequency (GHz)	Sl. No.	I/P Voltage(mV)	O/P frequency (GHz)
1	550	1.1511	14	1200	20.45952
2	600	2.144	15	1250	20.72324
3	650	3.75	16	1300	20.92926
4	700	5.91	17	1350	21.09883
5	750	8.45	18	1400	21.22781
6	800	10.978	19	1450	21.3402
7	850	13.2531	20	1500	21.438525
8	900	15.191	21	1550	21.51046
9	950	16.7692	22	1600	21.577766
10	1000	18.008	23	1650	21.630507
11	1050	18.9444	24	1700	21.6792767
12	1100	19.6186	25	1750	21.716941
13	1150	20.10454	26	1800	21.74291181

PHASE FREQUENCY DETECTOR

The transient response of PFD Fig.14 show that the UP output is high when feedback signal lags behind reference signal and the DOWN output is high at feedback signal leads the reference signal. Both the output are in zero potential at both inputs are logic high for the PFD schematic Fig.13

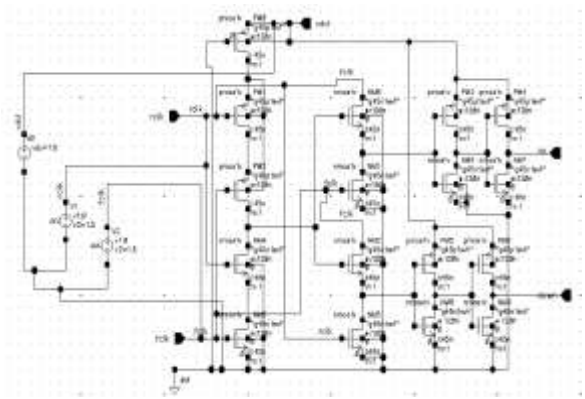

Fig.13 PFD design using cadence virtuoso

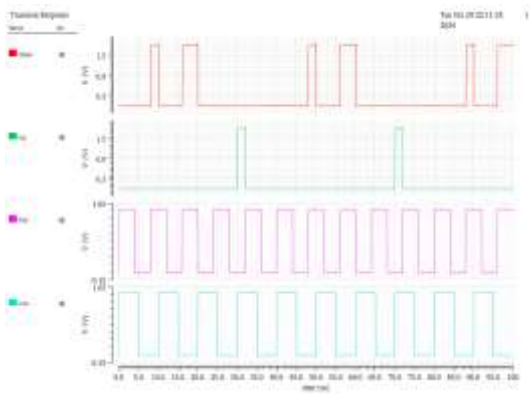

Fig.14 PFD transient response

PHASE DETECTOR

Figure.15 PD designed using cadence virtuoso and its transient response Fig.16 From the transient response analysis the tabulation Table.2 shows that the average output potential increases with respect to applied input frequency. It is suitable for applying as the input controlling voltage for CSVCO

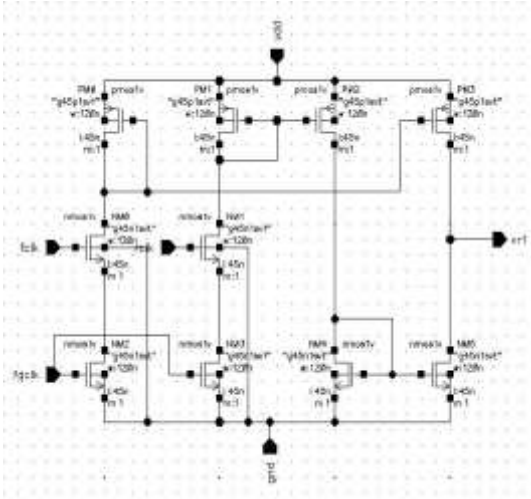

Fig.15 Phase Detector schematic Diagram

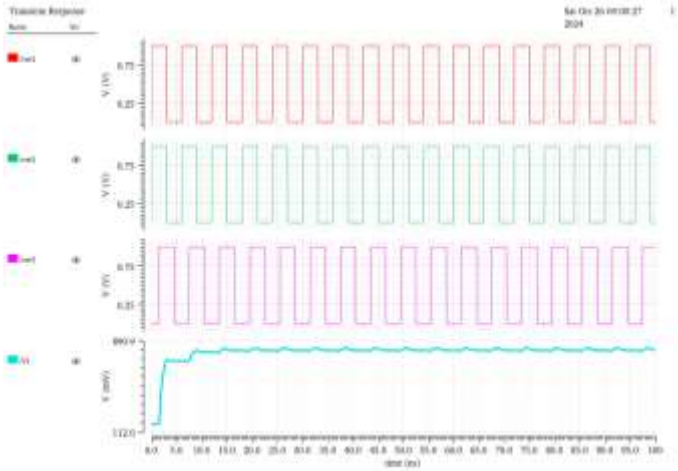

Fig.16 Transient response of PD

TABLE 2 Phase Detector analysis

SL.NO	I/P Time period (n sec)	I/P Frequency(MHz)	Average O/P (m Volt)
1	8	125.00	789.6
2	10	100.00	787.6
3	12	83.33	784.9
4	14	71.42	782.1
5	16	62.50	778.8
6	18	55.55	776.2
7	20	50.00	772.6

XII. ANALYSIS RESULTS OF MODIFIED DUAL-LOOP PLL

The results obtained from the analysis using Cadence Virtuoso 45nm technology for the modified dual-loop PLL architecture Fig.17 having low power consumption Fig.18 for Input Frequency: 72.46 MHz the Output Frequency: 18.55 GHz, Fig.20 Average Power Consumption: 499.1 µW, Maximum Power Consumption: 1.1057m W, Minimum Power Consumption: 228 µW and Fig.19 Jitter**:** 355 p sec, setup time for CSVCO and divide by N counter to produce feedback frequency output is 775n sec, total settling time of DL-PLL 1.2µ sec, The table 1 shows the wide oscillation capability of CSVCO ranges from 6GHz to 21GHz

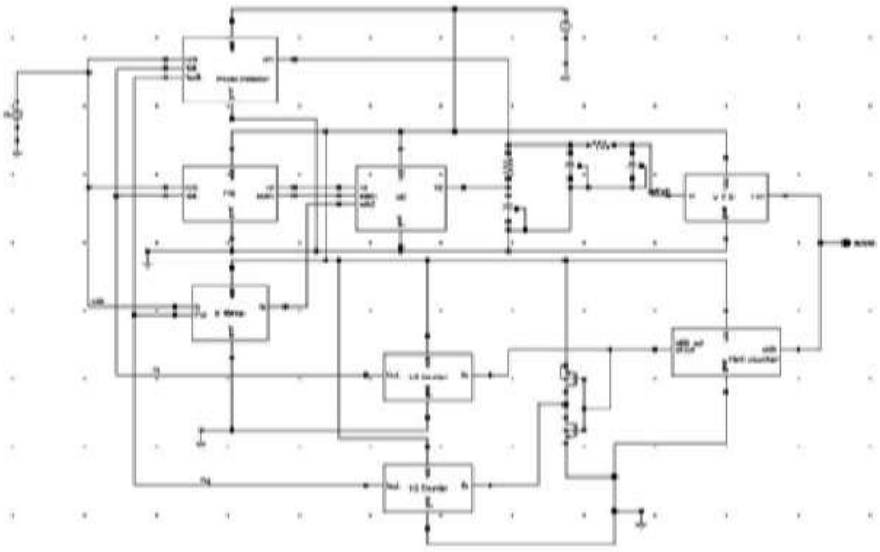

Fig.17 Modified Dual-loop Phase Locked Loop Schematic Diagram using cadence virtuoso

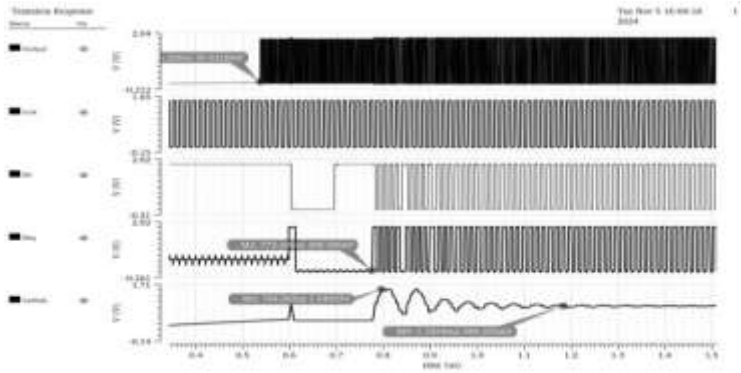

Fig.18 Transient Response of DL-PLL

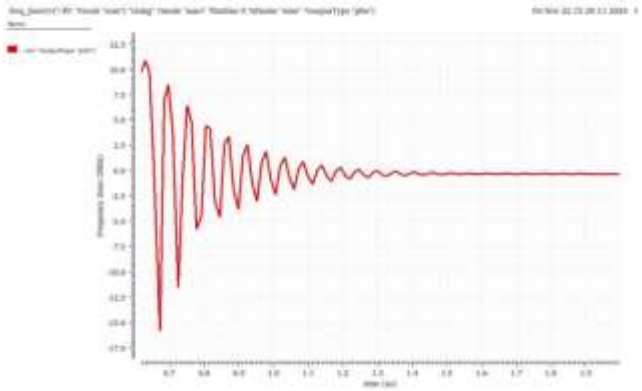

Fig.19 JITTER response

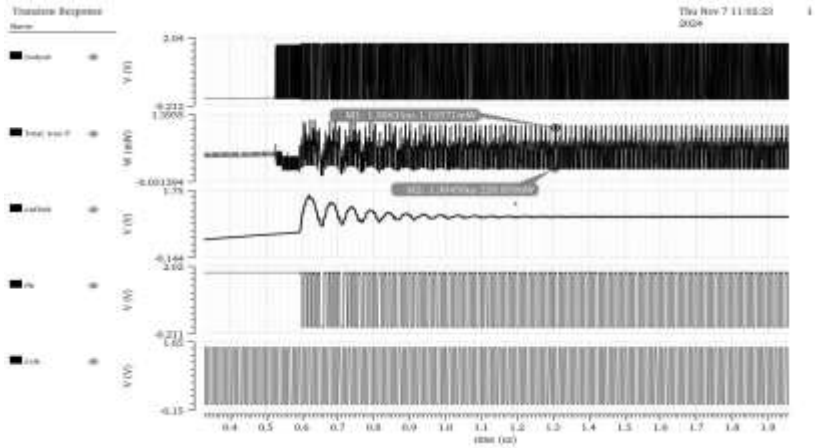

Fig.20 Power analysis

XIII. CONCLUSION

The future potential of the modified dual-loop PLL architecture lies in its ability to evolve with advancing technologies. By addressing the growing demands for higher-frequency performance, power efficiency, reduced jitter, and advanced synchronization, it will play a key role in the development of next-generation communication systems, data processing platforms, and more. Its versatility and adaptability make it a promising solution for a wide range of applications in wireless communication, IoT, high-speed computing, and other cutting-edge technologies.

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