HIGH SPEED CARRY SKIP ADDER IMPLEMENTATION USING AOI AND OAI BASED ON TRANSMISSION GATES

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***Abstract*: In this paper, a static CMOS CSKA structure called CI-CSKA was proposed, which displays a higher speed and lower energy utilization compared with those of the conventional one. The speed enhancement was achieved by modifying the structure through the concatenation and incrementation techniques. AOI and OAI compound gates were misused for the carry skip logic. The efficiency of the proposed structure for both FSS and VSS was studied by comparing its power and delay with those of the Conv-CSKA, RCA, CIA, SQRT-CSLA, and KSA structures. The outcomes uncovered significantly lower PDP for the VSS execution of the CI-CSKA structure over a wide range of voltage from super-threshold to near threshold. The result suggested the CI-CSKA structure as a generally excellent adder for the applications where both the speed and energy utilization are critical. In addition, a hybrid variable latency extension of the structure was proposed. The efficacy of this structure was compared versus those of the variable latency RCA, C2SLA, and hybrid C2SLA structures. Again, the recommended structure indicated the lowest delay and PDP improving itself as a possibility for high speed low-energy applications.**

***Keywords*: RCA, C2SLA, CI-CSKA, CSKA, AOI, IOA, Conv CSKA**

INTRODUCTION: Integrated circuit can see as a set of electronic circuits integrated on a small semiconductor, called as silicon chip. Very-large-scale integration (VLSI) began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. A limited set of functions could perform previously. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. Digital systems are designed to store process, and communicate information in digital form. They are found in a wide range of applications, including process control, communication systems, digital instruments, and consumer products. The carry skip adder requires less area when compared to the other adders like carry look ahead adder, carry select adder etc. Arithmetic addition determines the execution speed and performance of the entire calculation. MAC (Multiplier Accumulator) operations compute two numbers and add that product to an accumulator. Therefore, the functionality of the adder unit enables high speed processing of processors and DSP applications which helps in improving the performance of the system. Adder is one of the common and most critical component of a processor. Power consumption and delay are the major issues in the case of a processor. Usually, adder consists of number of basic gates. The performance of these adders plays a vital role in every processor. In this project, we designed a high performance carry skip adder by replacing the basic gates which are designed with conventional CMOS logic with Transmission Gate logic.

LITERATURE SURVEY: Over the past two decades advances in computer architecture have allowed the performance of digital computer hardware to continue its vast exponential growth. Despite increasing the difficulty in technology have wide speed improvement at the circuit level. This phenomenal rate of growth, which is expected to continue in the future, would not have been possible without theoretical insights, experimental research. In the computer designers lookup for user-friendliness, compactness, simplicity, high performance, low cost, and low power, computer arithmetic plays a key role.

2.1 Delay Efficient 32-Bit Carry-Skip Adder:
A new 32-bit carry skip adder that is divided into four variable width blocks is presented in this paper. The size of each block is limited by the delay of the carry-in signal and the final target delay. An algorithm is used to calculate the maximum size of the adder for the target delay. The group propogate group generate functions used in carry look ahead logic are used to speed up multiple stages of ripple carry adders.

2.2 Design Of High Speed And Low Power Carry Skip Adder Using Speculative Technique:
The enhancement of speed is achieved by applying concatenation and schemes to improve the good organization of the conventional CSKA (Conv-CSKA) structure. Instead of utilizing multiplexer logic, the arrangement introduces the working of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. Which lowers the power utilization without considerably impacting the speed, is presented. The efficiency of the proposed structure for equally FSS and VSS was studied by comparing its power and delay with those of the Conventional-CSKA, RCA, CIA, SQRT-CSLA, and KSA structures.

2.3 Combinational Circuits Using Transmission Gate Logic for Power Optimization:
International Technology Roadmap for Semiconductors (ITRS) states that leakage power dissipation may ultimately dominate total power consumption as technology feature sizes shrink. During the last two decades the idea to augment the performance of logic circuits results in the progress of many logical design techniques. Power and energy dissipation are reduced using transmission gate

logic (TGL), which are the challenging factors in the VLSI CMOS design. In order to get strong output level PMOS and NMOS are connected together.

2.4 4-Bit Brent Kung Parallel Prefix Adder Design Simulation Study Using SilvacoEda Tool:
The objective of this paper is to review the performance of the adder by forming different of transistors gate sizing and schematics. Here, the Brent Kung Adder was implemented in basic logic gates and compound gate, then simulated the design in various sizes of transistors in order to see the effect of propagation delay, power consumption and the number of transistors used.

2.5 Energy Efficient and High Speed Carry Skip Adder Operating Under A Wide Range Of Supply Voltage Levels:

The speed enhancement is accomplished by implication plans to improve the effectiveness of the regular CSKA structure. The hybrid variable latency augmentation of the proposed structure which brings down the power utilization without impressively affecting the speed is displayed. Recreations on the proposed mixture variable idleness CSKA uncover decrease in the power utilization contrasted and the most recent works in this field while having a sensibly fast.

III. CARRY SKIP ADDER:

A carry-skip adder skips the output carry of the ripple carry adder by using skip logic (multiplexer and XOR gates) which is used in the structure. This adder implementation improves the delay of a ripple-carry adder with little effort compared to other adders.

The most pessimistic scenario delay is accomplished by utilizing a few carry skip adders to shape a block carry skip adder known as carry by pass adder.

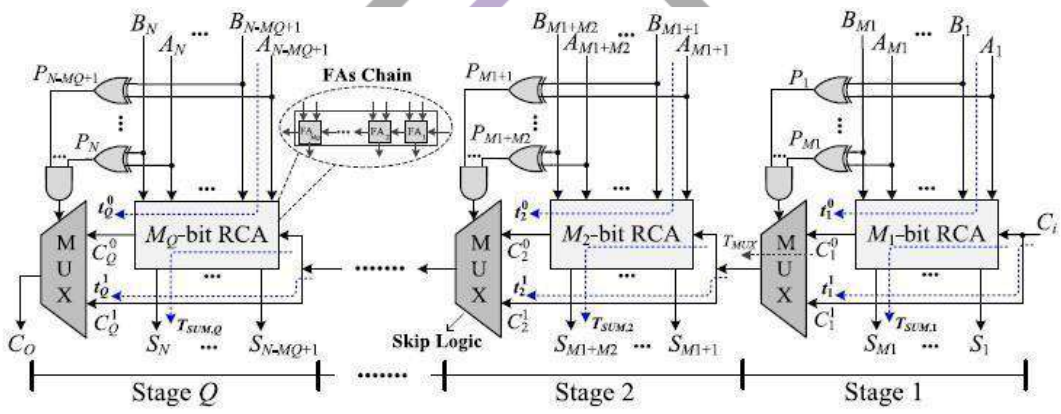

Figure 1: Conventional structure of the CSKA

There is a carry skip logic to the chain of FAs in each stage, For an RCA that contains N cascaded FAs, the worst propagation delay of the summation of two N-bit numbers, A and B, belongs to the case where all the FAs are in the propagation mode. It implies that the most pessimistic scenario delay has a place with the situation where

Pi = Ai Bi =1 for I = 1, . . . , N .....(1)

Here Pi is the propagation signal related to Ai and Bi. This shows the delay of the RCA is directly identified with N.

CSKA USING AOI AND OAI COMPOUND GATES:

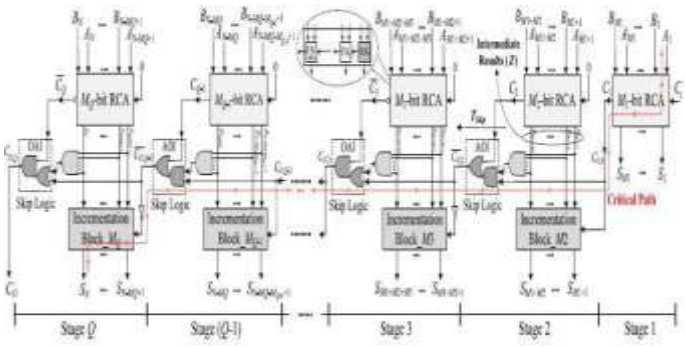

Figure 2: CSKA structure using AOI and OAI compound gates.

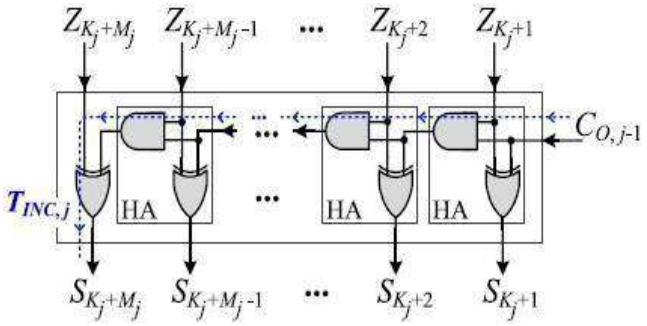

Figure 3: Internal structure of the jth incrementation block

IV. PROPOSED TRANSMISSION GATE TECHNIQUE

A transmission gate represents another class of logic circuits, which use transmission gates as basic building blocks. A Transmission Gate (T-gate or TG or pass gate) is a bi-directional switch made up of an NMOS and PMOS in parallel. A control signal is connected to the NMOS (C) and its complement is sent to the gate of the PMOS (C'). The T-gate is a bi-directional switch between A (input) and B (output) which is controlled by C (control signal).

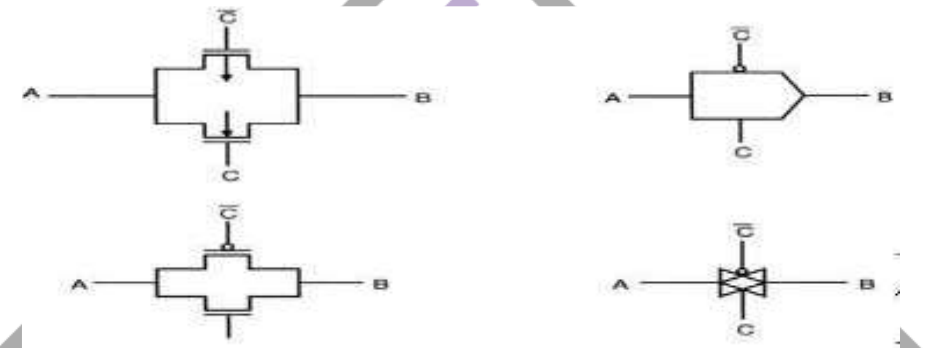

Figure 4: Schematic and logic symbol of Transmission gate

5.1 TRANSMISSION GATE CARRY SKIP ADDER:

We know that the carry skip adder consists of multiplexer, full adder, XOR and AND logic gates. If these gates are replaced with the gates which are designed using transmission gate logic then the number of transistors can be reduced which results in less power consumption.

The following figure represents the N-bit carry skip adder structure. The full adders, XOR logic gate, multiplexers in every stage are designed using Transmission Gate to reduce the number of transistors.

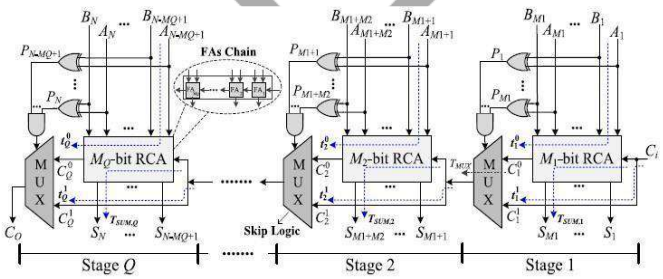

Figure 5: Structure of Transmission Gate Carry Skip Adder

VI. SIMULATION RESULTS

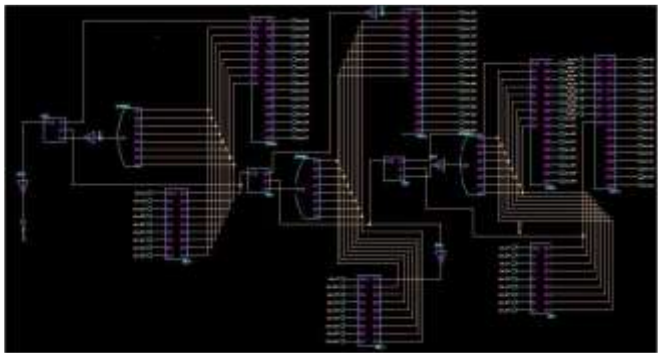

Figure 6: Schematic of conventional 32-bit CSKA using AOI and OAI compound gates

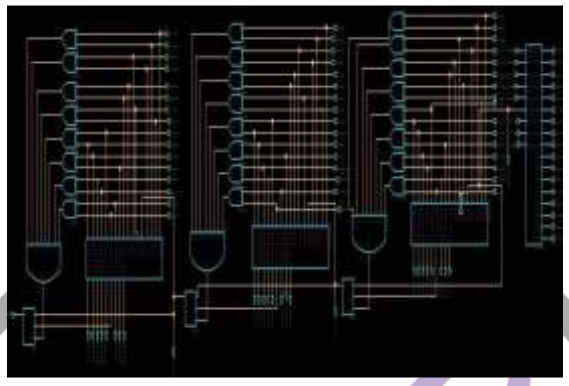

Figure 7: Schematic of 32-bit CSKA by replacing conventional XOR, MUX, full adder with Transmissions Gate logic

Table 1: Comparison of power consumption and delay values of different CSKA structures

Model	**Power Consumption**	delay
Conventional CSKA	2.4303 m watts	596.16 ps
CSKA using AOI and OAI gates	1.6854 m watts	351.04 ps
CSKA using PPA	29.380 m watts	350.19 ps
CSKA only by replacing with Transmission Gate full adder	2.0002 m watts	136.76 ps
CSKA only by replacing with Transmission Gate XOR gate	2.2494 m watts	455.20 ps
CSKA only by replacing with Transmission Gate multiplexer	2.0917 m watts	420.89 ps
CSKA using Transmission Gate in all components	3.0544 m watts	33.404 ps

VI. CONCLUSION

In this paper, a static CMOS CSKA structure called CI-CSKA was proposed, which displays a higher speed and lower vitality utilization contrasted and those of the ordinary one.

The speed enhancement was achieved by modifying the structure through the concatenation and incrimentation techniques. In addition, AOI and OAI compound gates were misused for the carry skip logics. The efficiency of the proposed structure for both FSS and VSS was studied by comparing its power and delay with those of the Conv-CSKA, RCA, CIA, SQRT-CSLA, and KSA structures. The results revealed considerably lower PDP for the VSS implementation of the CICSKA structure over a wide range of voltage from super-threshold to near threshold. The results also suggested the CI-CSKA structure as a needed adder for the applications where both the speed and energy consumption are critical. In addition, a variable latency extension of the structure was proposed. It misused a modified parallel adder structure at the middle stage for increasing the slack time, which provided us with the opportunity for lowering the energy consumption by reducing the supply voltage. The efficiency of this structure was compared versus those of the variable latency RCA, C2SLA, and hybrid C2SLA structures. Again, the suggested structure showed the lowest delay and PDP making itself as a better candidate for highspeed low-energy applications.

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