Performance analysis of 32 bit vedic multiplier design using nikilam and kogge stone adder

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***Abstract*: The multiplier speed is a necessary feature because the multiplier forms a vital part of several systems like FIR filters, microprocessors, DSPs etc. The multiplier is slow as compared to other parts of the system thus it is the speed determining factor of the system. An improvement in multiplier speed eventually end up in an improvement in speed of the overall system. The multiplier speed not solely depends on the multiplication technique used it additionally depends on the sort of adder employed for the addition of the partial product. The proposed work is relies on the vedic multiplication technique and high speed modified Kogge Stone adders are used. An 8 bit multiplier is complete victimization changed 4 bit multipliers which intern area unit complete victimization changed 2bit vedic multipliers. The design is simulated using Xilinx 14.7 software tool.**

***Keywords*: Vedic multiplier, Nikhilam sutra, Kogge Stone adder.**

1. INTRODUCTION

Multiplication is a vital elementary operate in arithmetic operations. Multiplication-based operations such as multiply and Accumulate (MAC) unit and inner products are some of the frequently used Computation- Intensive Arithmetic Functions presently enforced in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform (FFT), filter circuits and in microprocessors in its arithmetic and logic unit (ALU).

Since multiplication dominates the execution time of most DSP algorithms, therefore there is a necessity of high speed multiplier. Currently, multiplication time is still the dominant consider deciding the instruction cycle time of a DSP chip. During this work we have got place into effect a high speed Vedic multiplier using barrel shifter. The sutra was implemented by changed style of "Nikhilam Sutra" due to its feature of reducing the amount of partial products. The barrel shifter is employed at totally different levels of designs to scale back the delay when compared to conventional multipliers. The hardware implementation of Vedic multiplier is using barrel shifter contributes to adequate improvement of the speed. In several DSP algorithms, the multiplier lies within the critical delay path and ultimately determines the performance of algorithmic program. The speed of multiplication operation is great importance in DSP similarly as generally in processor. In past multiplication was enforced with a sequence of addition, subtraction and shift operations. There are several algorithms proposals to perform the multiplication, and each offering different advantages and having in terms of speed, circuit complexity, area and power consumption. The multiplier could be fairly gaint block of a computing system. For multiplication algorithms performed in DSP applications latency and throughput are the two major concederations from delay perspective. Latency is that the real delay of computing a function, a measure of how long the inputs to a device are stable is that the conclusion obtainable on outputs.

Throughput is that the measure of how many multiplications may be performed during a given period of time multiplier is not solely a high delay block however conjointly a serious supply of power dissipation. That's why if one also aims to minimize power consumption, it is of great interest to scale back the delay by using various delay optimizations. Advanced multipliers are the centre components of all the computerized signal processors (DSPs) and therefore the rate of the DSP is usually controlled by the velocity of its multipliers. Two most elementry duplication calculations followed within the computerized equipment are exhibit increase calculation and Booth augmentation calculation.

The calculation time taken by the exhibit multiplier is comparatively less on the grounds that the halfway items are ascertained autonomously in parallel. The postponement connected with the exhibit multiplier is that the time taken by the signs to unfold through the entryways that shape the Multiplication cluster. Corner increase is another important augmentation calculation. Extensive corner clusters are required for quick duplication and exponential operations that so need expansive halfway aggregate and incomplete convey registers. Duplication of two n-bit operands utilizing a radix-4 corner recording multiplier needs roughly n/(2m) clock cycles to form the minimum noteworthy portion of the last item, where m is that the quantity of Booth recorder snake stages. Hence, an in depth unfold deferral is connected with this case.

2. PREVIOUS WORKS

This half is concerning the connected work supported adders and multipliers. "Design and Implementation of Vedic Multiplier" was proposed by C.Sheshavali and K.Niranjan kumar . Therefore the proposed multiplier provides higher performance and results for higher order bit multiplication. during this multiplier higher order bit multiplication from 16 x 16 bit and more than that value is applicable, the multiplier is complete by instantiating the lower order bit multiplier. This is mainly due to memory occupied by each operation. Effective memory implementation and preparation of memory compression algorithms will yield even higher results.

Pushpalata Verma proposed an "Implementation of an Efficient Multiplier based on Vedic Mathematics Using EDA Tool". This paper may be a extremely economical technique in multiplication – "Urdhva Tiryakbhyam Sutra" is one of the method Vedic mathematics. It provides hierarchical multiplier design and clearly indicates the computational advantages offered by Vedic methods. The trail delay that is measure for the computation proposed 8x8 bit Vedic multiplier is found to be 21.679ns. Thus our motivation is consumed and the delay is reduced. Therefore, we tend to discover that the Vedic multiplier is little bit efficient in terms of execution time (speed) than Array and Booth multiplier factor. The benifits of the vedic multiplication will be enclosed as a awareness for the multipliers. In future, all the major universities might create 2244 acceptable analysis centers to promote research works in Vedic mathematics.

Poornima M, Shivaraj Kumar Patil, Shivukumar proposed "Implementation of Multiplier using Vedic Algorithm".This paper presents a extremely economical method for multiplication – "Urdhva Tiryakbhyam Sutra" that relies on Vedic mathematics. It is a way for hierarchical multiplier created to indicate the benefits of computational delay offered by Vedic methods. Authors enforced the code on Xilinx FPGA Spartan 3A board .Computational path delay for our proposed 8x8 bit Vedic multiplier is found to be 28.27 nano seconds. It has been discovered that the Vedic multiplier is much more efficient in terms of execution time (speed) than Array and Booth multiplier factor. An awareness of Vedic mathematics concepts will be effectively accrued if it is enclosed in engineering education.

G. Ganesh Kumar, V. Charishma proposed "Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques". The designs of 32x32 bits Vedic multiplier have been proposed by using Spartan XC3S500-5-FG320. The look relies on multiplication in vedic methods[3]. The worst case propagation
Delay within the Optimized Vedic multiplier case is 31.526ns. However proposed adder in this paper is little bit better than the the conventional multipliers. This paper and technique shows the steps and also the manner of the technique to form hierarchical multiplier design. Therefore the design complexity gets reduced for large number of bits as input and modularity can get accrued.

Urdhva tiryakbhyam, Anurupye and Nikhilam sutras are such algorithms which can reduce the power delay and hardware necessities used for multiplication of numbers. FPGA implementation of this multiplier shows that method to analyse the hardware necessities and operations of the Vedic mathematics algorithms is feasible. The high speed multiplier algorithm exhibits is improved in terms of speed.

3. NIKILAM SUTRAM

Nikhilam is one of the 16 sutra from Vedic Mathematics. This sutra is employed to convert large- digit multiplication to tiny digit multiplication using few subtract, add, and shift operation. Steps for multiplication of 2 digit number which are less than the nearest base using Nikhilam sutra are as shown in table 1.

Step 1	$a \times b$
Step 2	$A = (\text{Nearest base}) - a$
Step 3	$B = (\text{Nearest base}) - b$
Step 4	$C = A \times B$
Step 5	$D = a - B = b - A$
Step 6	$Result = 100 \times D + C$

The net advantage is that it reduces the requirement of microprocessors to control at more and higher clock frequencies. While a better clock frequency typically ends up in multiplied processing power, its disadvantage is that it conjointly increases power dissipation which ends up in higher device operational temperatures. The process power of multiplier will simply be increased by increasing the input and output data bus widths since it is a quite a regular structure. Due to its regular structure, it may be simply layout during a silicon chip. The Multiplier has the advantage that because the verity of bits will increase, gate delay and space will increase very slowly as compared to alternate multipliers. Therefore it is time, area and power economical.

4. KOGGE STONE ADDER

Adders form an essential component of the multipliers, in fact the speed of the multiplier to an oversized extent depends on the speed of the adder. Different kinds of adders with totally different space to delay tradeoff are present. Our aim is to pick the adder that provides the simplest tradeoff between the realm occupied by it and therefore the delay that it introduces. KSA is predicated on the thought of parallel prefix computation. The G and P values out lined in Carry look ahead adder are combined in kogge stone adder before getting used. On combining two columns along the unit propagates a carry bit on condition that each right and left column propagate. However it generates a carry even when only one column generates and the other propagates.

Gunit = G1+ P1.G0

Punit=P1.P0

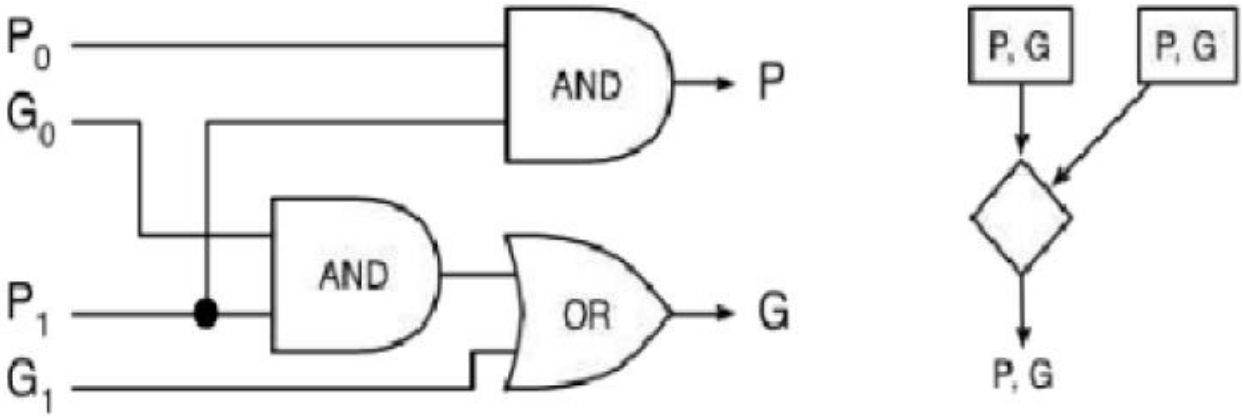

Fig 1. Carry propagation and generation unit [4]

Thus by performing recursive combinations we can compute final carry in an 8 bit adder in 3 steps.

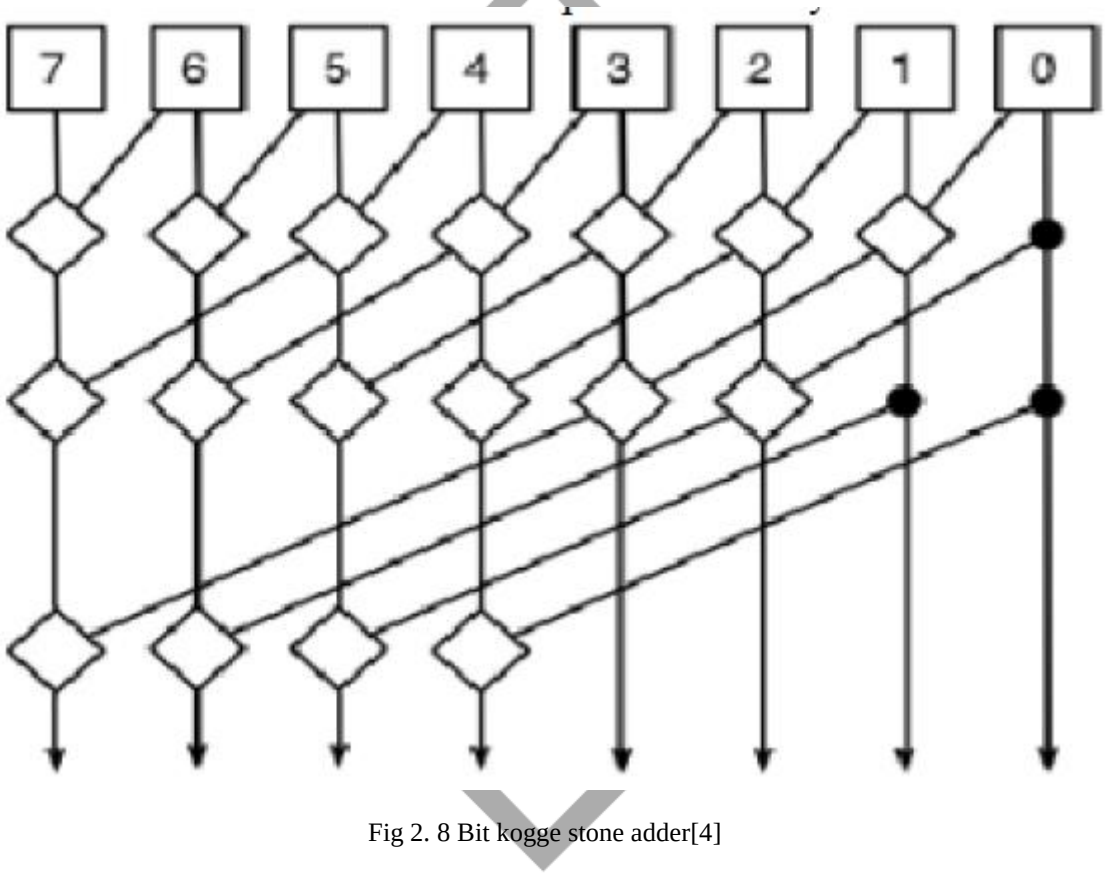

Fig 2. 8 Bit kogge stone adder[4]

The top square blocks with numbers represent the computed P and G bit of the eight columns of the 8 bit adder .Two adjacent set of columns are combine in the diamond formed blocks and thus a new combined P and G for the set is produced. At bottom the combined P and G for a selected column and each column to its right is represented by the arrows.

Cn= Gn-combined + Pn-combined .

Cin , Sn= Pn exor Cn-1

Kogge stone is the fastest doable layout as it scales logarithmically.

5. VEDIC MULTIPLIER USING KS ADDER

The multiplication of two numbers is finished by exploration Urdhwa Triyakbhyam. Here first the least significant bits of the two digits are multiplied. Then the intermediate digits are cross multi-plied and added together. After this the foremost significant digits are multiplied. For the 16X16 bit multiplication small block of 2X2 or 4X4 or 8X8 multiplier were used in parallel to form the method easy and efficient. In our proposed methodology the high speed carry select adder is replaced by the carry select adder together with Kogge Stone (KS) adder that claims to supply an improved speed and less propagation delay. Here we have got

used four multiplier of 8 bit to perform 16 bit multiplication. The strategy used is that the addition of all partial product finished by the cross multiplication of one bit with another. The LSB bits of first multiplier P1 (7-0) gives the LSB bits Q (7-0) of the final output. Another bits of first multiplier P1 (15-8) are added in series with LSB 8 bits of second multiplier to form the 16 bits, that successively get another with 16 bits of third multiplier by using KS Adder. The LSB bits of the output of KS adder forms the Q (15-8) bits of the final output. The remaining 8 bit P2(15-8) is then added with the left 8 bits of KS output to from 16 bits, which is then added with 16 bits of the fourth multiplier by using KS 2 adder. The output from KS 2 adder forms the Q (31-16) bits. This is how the 32bit output is achieved with in the less donable time.

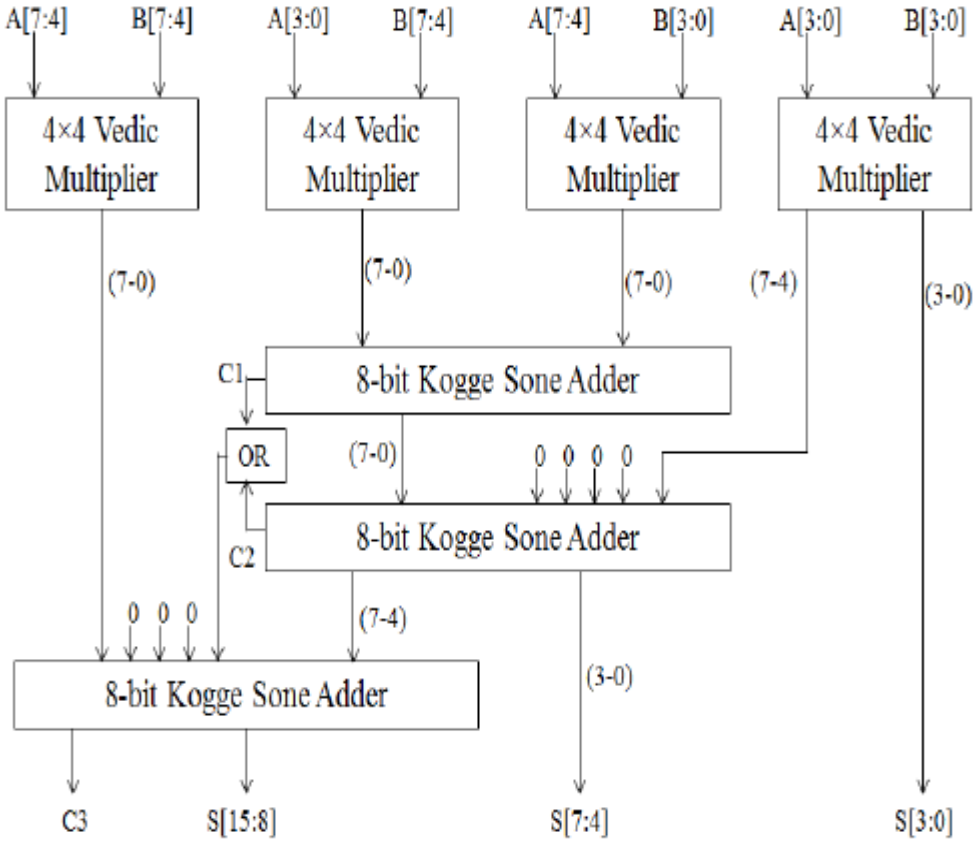

Fig 3: Logic Diagram of Vedic Multiplier using Kogge Stone Adder

6. SIMULATION RESULTS

The results obtained for vedic multiplier using kogge stone adder are shown below.

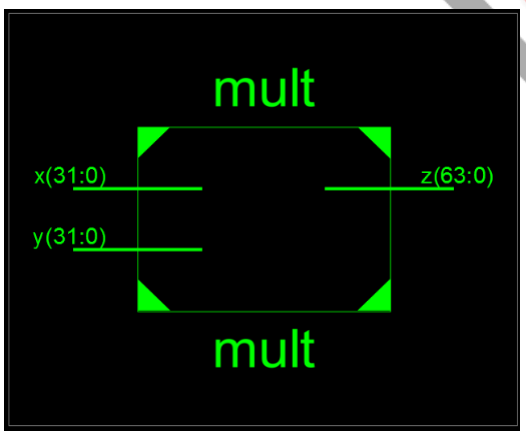

Fig 4: RTL Schematic

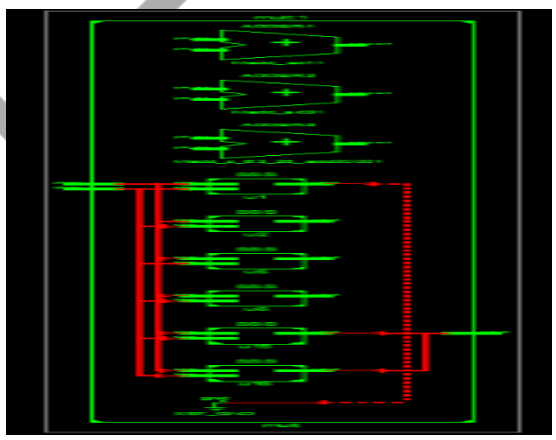

Fig 5. Technological Schematic

The simulation output for 32 bit inputs, with a 64bit output is shown below.

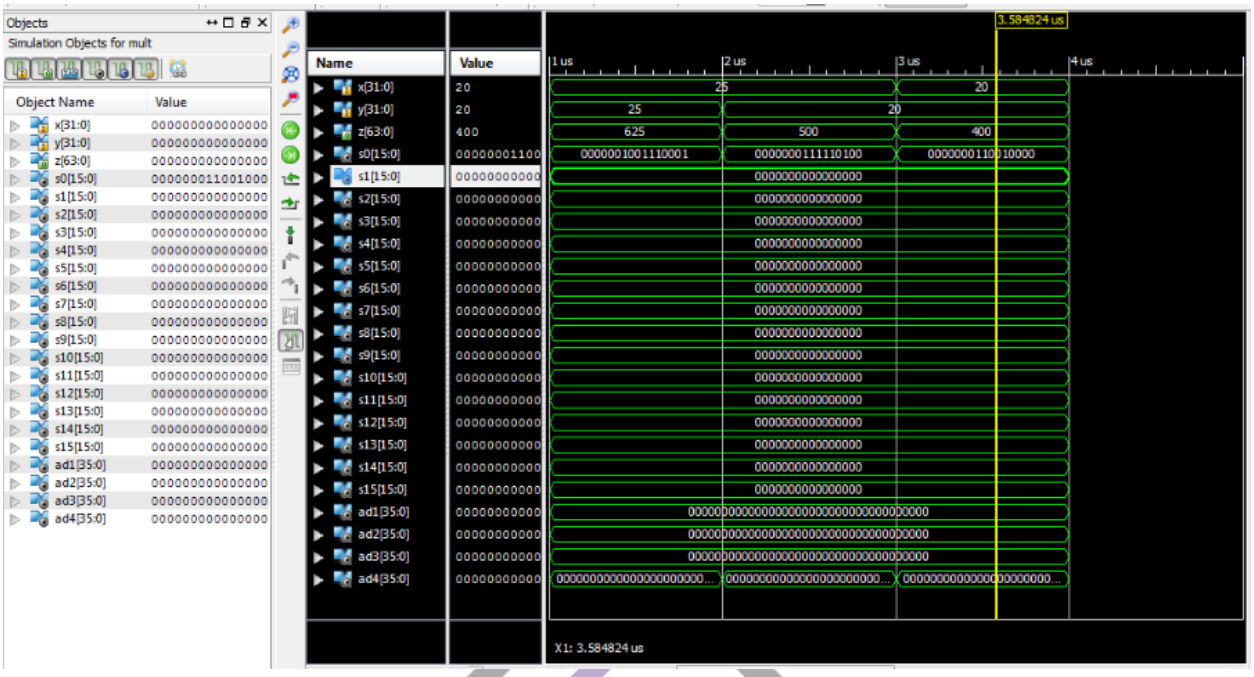

Fig 6. Simulation Output

The temporal order report is obtained and the time taken to complete the process is 26.532 ns

7. CONCLUSION

As Nikilam Vedic multiplier is synthesized using totally different adders in past, we have a tendency to planned a KSA and it is ascertained that kogge stone adder provides the best response in terms of speed, i.e. time delay is minimum while using kogge stone adder. Further, a more symmetric architecture for a Vedic multiplier is enforced. Modified lower order multipliers and modified kogge stone adders have then been accustomed additional cut back the delay and the area occupied. For future work 16x16 and alternative higher order multipliers may be designed using alternative high speed adders , the architecture can be worked on to further reduce the delay or the area occupied.

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