Analysis of Competitors' Products and Development of a High-Performance Mixer

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***Abstract*: In more recent times, there has been a significant rise in the application of the RF mixer. Because it offers high conversion gain, superior port-to-port isolation, and minimal even-order distortion, the Gilbert cell is often utilized as the heart of the mixer. It has been discovered that the Multi-Tanh technique improves the linearity of mixers by incorporating multiple differential trans-conductance stages; however, this results in a very low conversion gain. On the other hand, the use of the current bleeding technique improves both the linearity and conversion gain of mixers by increasing the bias current through the addition of a current source; however, this comes at the expense of increased power consumption. Because of the many benefits that CMOS technology offers, including cheap cost, low static power dissipation, and low space, it was the technology of choice for the creation of a low noise amplifier. This was due to the fact that CMOS technology has become the preeminent form of the technology. The single ended and differential LNA were built to work in a WCDMA reception range utilizing a BSIM3V2 model (Level 49) CMOS UMC 0.18m technology in Xcircuit Open source EDA tool. This enabled the LNAs to function inside the WCDMA reception range. Gain, noise, and linearity were all taken into consideration as some of the most important aspects of the design. The linear noise amplifiers (LNAs) were developed with the goals of providing high gain, matching to a 50 ohm RF system, and strong linearity.**

***Keywords*: Ultra-wideband (UWB), Differential mode of application, cross coupled feedback, Direct –Coupled amplifier.**

1. NTRODUCTION

The demand for wireless communication has been highest in the recent decade. High-frequency Trans receiver needs have been erratic and unpredictable.
In order to compete, wireless devices need to be cheap, efficient, fast, and plentiful. Integrated circuit (IC) technology advancements have resulted in ever smaller electronic components such as transistors. Increases in unity gain, cut of frequency (ft), and maximum operational frequency (Fmax), as well as a decrease in channel length, demonstrate the promise of CMOS in the RF system's front end [1]. As supplyvoltages drop, designing analog RF circuits becomes increasingly difficult. However, passive components like resistors, capacitors, and inductors are often used to construct RF circuits, and their sizes do not increase linearly with circuit size. This means that the chip's surface area doesn't shrink as much. To reduce the amount of silicon required and the associated costs, it is necessary to construct a trans-receiver on a single CMOS chip. Although certain digital processing operations have been intended to be as near to the front end as feasible, most RF front end components, including low noise amplifiers and mixers, are still developed in the analog domain. Channel lengths and widths continue shrinking as component technology improves. The super hetero dyne design [2] is the most common architecture in current RF receivers since the transistor uses less silicon space and switches quickly. A low noise amplifier (LNA) is the second part of a wireless receiver's front end. Its primary role is to provide a low-noise signal amplification for use in subsequent stages [3].

A mixer is the third part of the receiver's front end. The entering radio frequency (RF) signal is converted to the intermediate frequency (IF) via the mixer. Multiplying the LO frequency causes the output to be a series of mirror reflections of the original signal.

There are two main types of mixer: active and passive. The primary difference between the two types is conversion gain. When compared to their passive counterparts, active mixers have a higher conversion gain and use less power from the local oscillator (LO) [4]. Active mixers are often employed in RF applications because of their ability to decrease the noise introduced into following stages of the receiver. On the other side, passive mixers have high LO power needs and may be slow during conversion, but they have great intermodulation (IM) performance and are widely used in microwave and base station circuits [5].

The receiver front end has seen a number of active mixing types offered. The topology for a Gilbert cell mixer that can handle a resistive load is presented in this thesis. They performed well in terms of linearity and gain.

II. REVIEW OF TECHNIQUES

The 2.4 GHz frequency range is often utilized in a variety of communication technologies. This frequency range is used by the Wireless Local Area Network (WLAN) 802.11b standard and Bluetooth. The majority of today's communication networks adhere to this standard. Trans-receivers compatible with this frequency standard are desperately needed [4].

The receiver design is quite similar from an RF front end perspective. An integral part of any and all receiver architectures, the LNA and mixer. This thesis's discussions about mixer design are generally relevant to other types of receiver architecture as well. Unless the LNA's load is an external filter, in which case the LNA's performance must be assessed independently and the LNA's output must correspond to specific inputs, the mixer is the intermediate sub system that comes after the LNA [5].

Because of their superior switching characteristic, CMOS circuits are a need in digital circuit design. As a result, CMOS technology has become the standard in the VLSI industry for digital circuits. Because of its flawless switching characteristics. Switch-based high-performance mixers, or MOS passive switching mixers [6], have been created using metal-oxide-semiconductor (MOS) transistors. The MOS passive switching mixer makes use of four transistors that are each driven by an out-of-phase signal. Therefore, at any one moment, only two transistors powered by the same phase signal are active. If the input LO+(OR LO-) is big enough, the transistors can be switched perfectly ON or OFF without any losses.

The voltage gain of a mixer is equal to for a perfect square wave input signal.

The linearity performance of a MOS phase shift switching mixer is very high [7]. The use of a bias current is unnecessary. The homodyne trans-receiver greatly benefits from this quality. However, this style of mixer does have a few limitations. To flip the transistor completely ON or OFF, a high voltage drive is necessary. High levels of LO-RF and RF-IF feedthrough are caused by coupling through the gate-to-source capacitor.

In [8], a mixer design for low power receivers based on a source follower is shown. Using an unbalanced source coupled pair operation, the linearity of this mixer is exceptional. However, there is no gain and a significant feed through from the LO-IF. When compared to a passive switching mixer, this one doesn't perform all that well.

Using the disk-shaped GaAs Schottky diodes produced on a n/n+ epitaxial structure, we describe a high-performance single-balanced monolithic millimeter-wave integrated-circuit (MMIC) mixer operating at 94 gigahertz with a single balanced input [9]. The mixer displays a conversion loss of 5.5 dB at 94 GHz, a 1-dB compression point (P 1 -dB) of 5 dBm, and good local-oscillator to radio-frequency isolation of over 30 dB in an RF frequency range of 91-97 GHz. These results are made possible by the superior properties of the GaAs diodes, which have high diode-to-diode uniformity. To the best of our knowledge, the mixer that was manufactured has the greatest performance in terms of conversion loss at 94 GHz and P 1 -dB among the W-band MMIC mixers that do not have amplifier circuits.

Using the MOS transistor's body terminal for the mixing process is another viable option [10]. The term "Body Injection Mixer" describes this particular blender. By decreasing the number of stacked transistors, the supply voltage may be lowered. A noisy input to the body terminal results in a low conversion gain and poor noise performance.

III. PROPOSED CIRCUIT DESIGN

The antenna's radio frequency signal, boosted by a high-frequency low-noise amplifier. For digital signal processing, it is necessary to digitize these signals. Signals are down converted to lower intermediate frequencies (IF) before being sent on to the next stage of the signal processing chain. In order to generate a differential output signal, a Gilbert mixer is used here.

UMC's 180nm CMOS technology was used to create an active double-balanced CMOS Gilbert cell mixer. For high-frequency performance, the designers opted for an all NMOS Gilbert cell structure. Differential inputs are available on the double balanced mixer. The mixer accepts differential inputs on both the RF and LO ports to improve noise performance [11]. In order to lower the voltage supply demand even more, the NMOS transistors in the mixer core are biased close to their threshold voltage. We can see the individual numbers in Table 3.1. Transistor RF models were used for the Gilbert cellMixer.

Table 3.1: Component value for Mixer Design

.

Component	Value
Lall transistor	0.18µm
WM2, M3, M8, M11	25µm
WM4, M8, M12	105µm
R6, R7, R8	650,650,750Ω

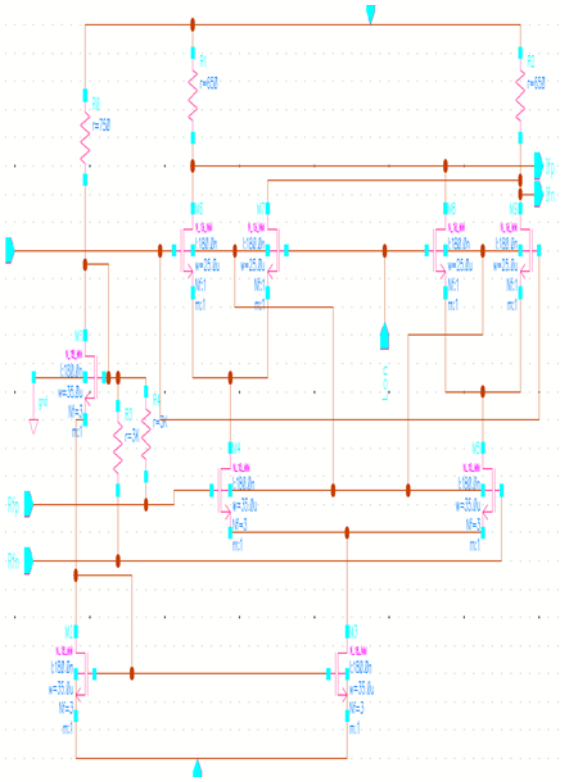

Figure 3.1: Schematic of Proposed Mixer with Biasing Circuitry

Bias current for the mixer core and the output buffer stage is adjusted by current mirror via transistor M7-M8 (see Figure 3.1 for the full mixer circuit with biasing circuitry). In order to combine the differential RF and LO signals, the V-I conversion is performed by transistors M6 and M7. The frequency conversion is accomplished by switching on and off transistors M1, M2, M3, and M4. For high-frequency use, a 650 Resistive load was used for.

The test setup for the proposed mixer is shown in Figure 3.2. In which the Gilbert cell mixer sign is linked to further diagnostic hardware. Here, a voltage source (port2) connects directly to the LO port of the Mixer in order to deliver the input LO voltage at a frequency of 2.25GHz [12]. The balun, which supplies the differential input RF signal from a single source (port1), is linked to the mixer's RF port. Port3 is used for monitoring the IF signal at the output. The power source for the mixer is 1.8V.

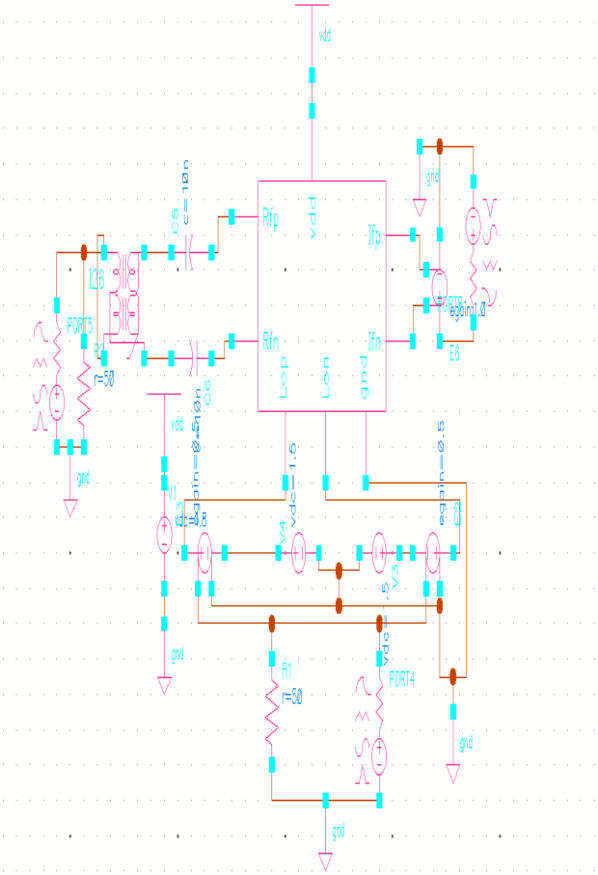

Figure 3.2: Test Bench for Proposed Mixer

3.1 Proposed Flow Chart

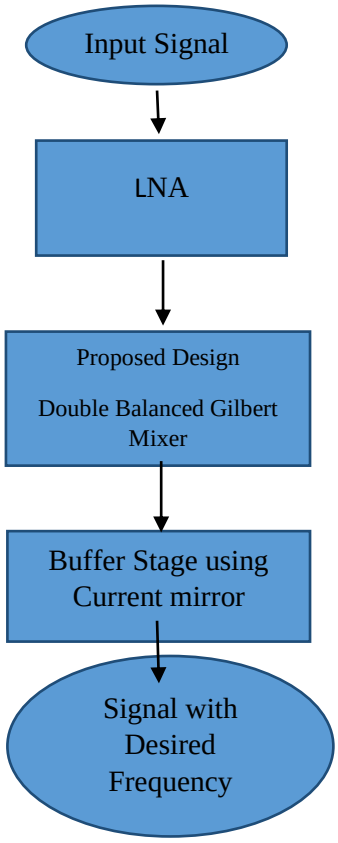

Figure 3.3: Proposed FlowChart

Topology for mixers is proposed. In order to boost the signal without introducing unwanted noise, we used a low-noise amplifier (LNA) in the first stage and followed it up with a mixer to get the desired frequency range [13]. In order to maintain a steady current, a buffer circuit or current mirror is utilized last.

Algorithm:

1) Solicit low-amplitude, fixed-frequency user input
2) Using a low-noise amplifier (LNA) to boost the signal.
3) A block of Gilbert cells are mixed together. Gilbert cell mixers, also known as Gilbert cell multipliers, are a kind of double balanced mixer that use cancellation of the RF and LO output signals to eliminate them from the intermediate frequency (IF).
4) Cascode amplifier formation for high gain.
5) Using a current mirror to maintain a steady current

IV. SIMULATION RESULT OF MIXER

Magic Simulator is used to model the mixer circuit. The mixer is calibrated for a voltage of 1.8V. The suggested mixer's simulation results are shown in Figures 4.1 to 4.8. As can be seen in Figure 4.1, the measured voltage conversion gain Swept PSS with PAC is around 6.7dB. Input and output impedance of the mixer are both set to 50, and the noise figure of the mixer was measured to be 15.5dB figure 4.2.

The effectiveness of linearity is evaluated using a two-tone test.The RF inputs of a mixer receive a second signal. The first input signal frequency is 2.4GHz, whereas the second is 2.401GHz the RF signal frequency. Boy basic output power and third order intermodulation distortion power as a function of input power are shown as a simulation result in Figures 4.1 and 4.2. The Input-referred IP3 plot at 1.5 dBm is displayed in Figure 4.3, and the 1-dB compression point is located at -11 dBm in Figure 4.4. The mixer has a low power requirement of around 10.0 mW at 1.8V.

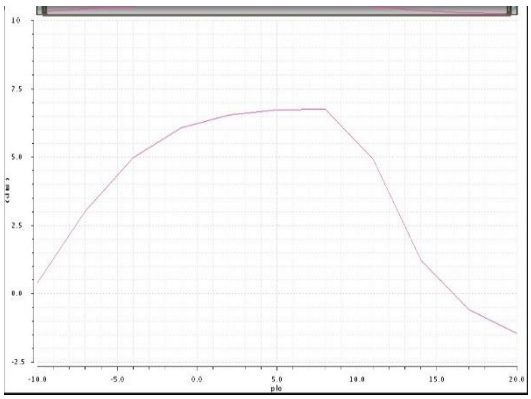

Figure 4.1: Conversion Gain of Proposed Mixer (Swept PSS with PAC)

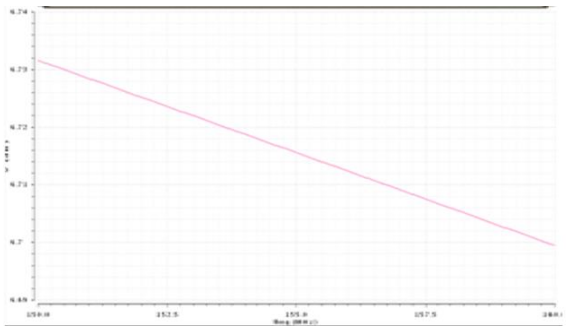

Figure 4.2: Conversion Gain of Proposed Mixer (PSS with Swept PAC)

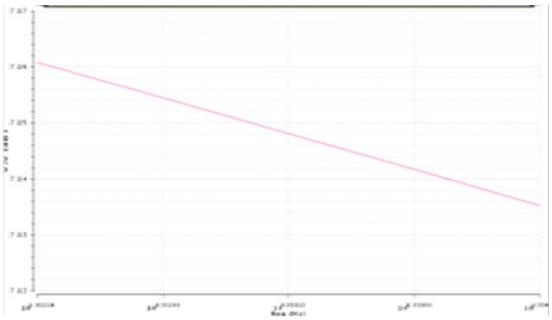

Figure 4.3:Conversion Gain of Proposed Mixer (PSS with Swept PXF)

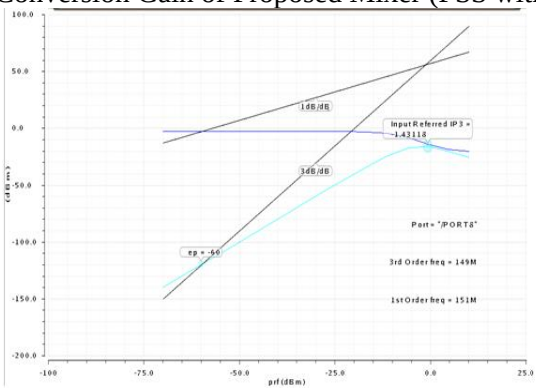

Figure 4.4: Third Order Intercept point

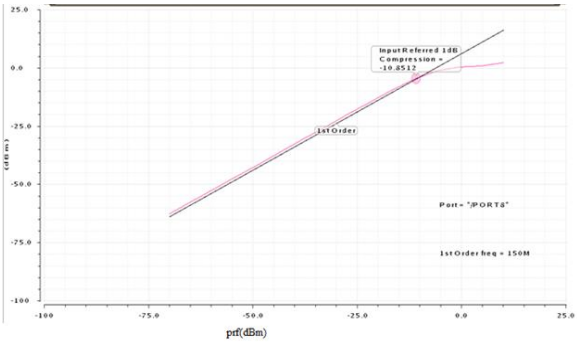

Figure 4.5: 1dB Compression Point

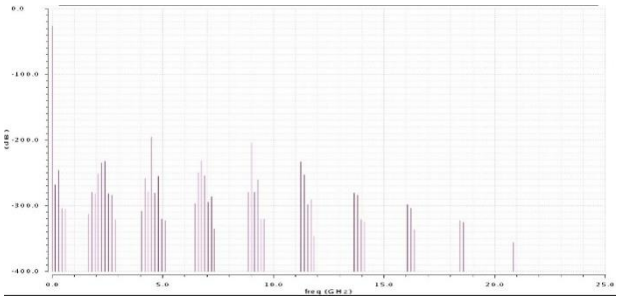

Figure 4.6:Power Consumption of a Proposed Mixer

4.1 Two Input Transconductance Stage Of The Proposed Mixer

Bipolar transistors and the multi-tanh concept are presented by Barrie Gilbert.In order to increase linearity and gain, this thesis use the multi-tanh method to develop a novel Structure. Let's start by multiplying by two [14]. The design used a 2.4GHz, 1.8V power supply, and a Trans conductive level with four NMOStransistors constructed in a UMC 0.18um CMOS process. Below is a breakdown of the parts and how much they're worth:

Table 4.1: Components value for Two input Trans conductancestage Mixer

Component	Value
LAll Transistor	0.18 µm
WM-M1,M2,M3,M4	80µm
WM-M5,M6,M7,M8,M9,M10,M11,M12	120µm
LoadResistor-R1,R2,R3	500Ω

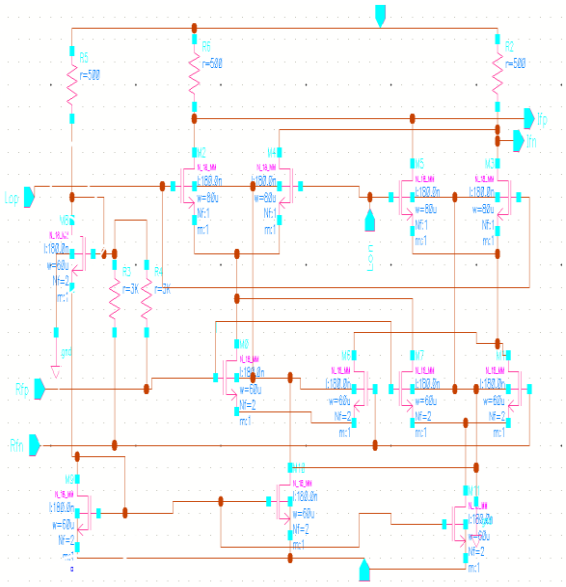

Figure 4.7: Schematic ofDouble Trans conductance stage Mixer

The bias current for the mixer core and the output buffer stage is controlled by a current mirror through transistors M10, M11, and M12. This circuit is seen in figure 4.7. In order to combine the differential RF and LO signals, the M6-M7-M8-M9 transistors execute a V-I conversion. The frequency conversion is accomplished by switching on and off transistors M1, M2, M3, and M4. For high-frequency work, we've settled on a 500 Resistive load.

The test setup for the proposed mixer is shown in Figure 4.8. Wherein the Gilbert cell mixer icon is linked to a supplementary circuit for studying the mixer [15]. Here, a voltage source (port2) connects directly to the LO port of the Mixer in order to deliver the input LO voltage at a frequency of 2.25GHz.

The balun, which supplies the differential input RF signal from a single source (port1), is linked to the mixer's RF port.Port3 is used for monitoring the IF signal at the output. The power source for the mixer is 1.8V.

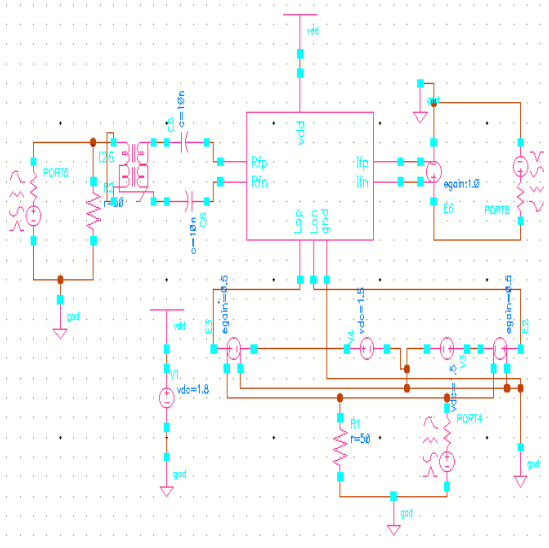

Figure 4.8: Test Bench of Double Trans conductance stage Mixer

4.2 Simulated Result Of Mixer

Spectra-RF simulator is used to mimic the mixer circuit in the magic simulator. The mixer is calibrated for a voltage of 1.8V. The simulation results of the suggested mixer are shown in Figure 4.9 through Figure 4.12. Figure 4.9 displays the approximate 12.5dB increase in voltage conversion that was measured (Swept PSS with PAC). Figure 4.9 displays the noise figure of the mixer, which was measured to be 15.5 dB [16]. The mixer's impedance is set to 50 on both the input and the output.

The effectiveness of linearity is evaluated using a two-tone test.The RF inputs of a mixer receive a second signal. Both the first and second input signals have a frequency of 2.401 GHz, with 2.4 GHz being the RF signal frequency. Double transconductance stage mixer conversion gain is seen in Figure 4.9. Figure 4.10 depicts the plot of the Input-referred IP3 measured to -1dBm, while figure 4.11 depicts the 1-dB compression point being located at -10dBm. The mixer has a low power requirement of around 10.0 mW at 1.8V.

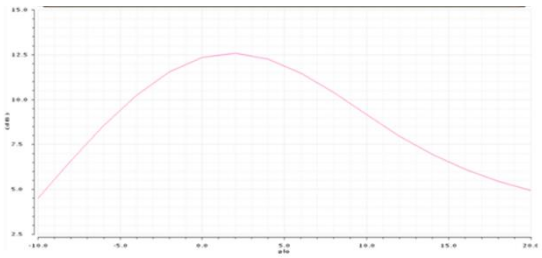

Figure 4.9: Voltage Conversion Gain (swept PSS with PAC)

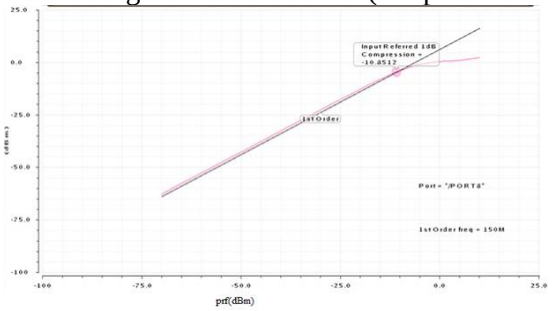

Figure 4.10: 1dB Compression poin

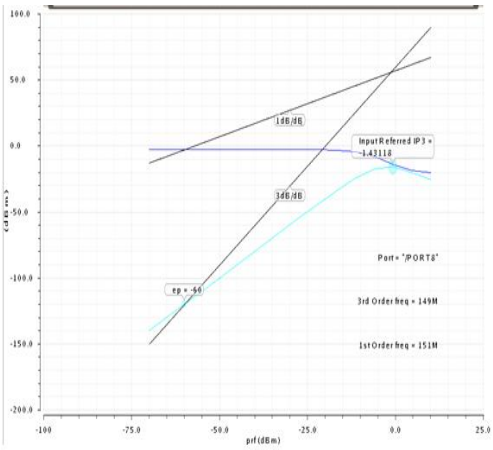

Figure 4.11: Third order Intercept Point

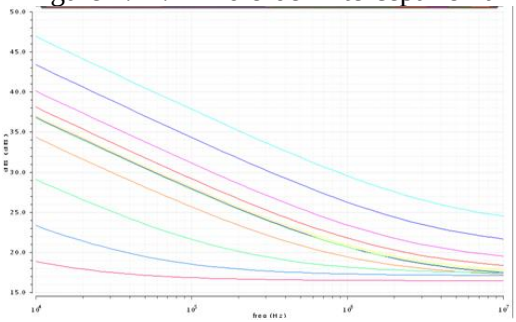

Figure 4.12: Noise Figure of Proposed Mixer

4.3 Three input Transconductance stage of the Proposed Mixer

Bipolar transistors and the multi-tanh concept were proposed by Barrie Gilbert. In order to increase linearity and gain, this thesis use the multi-tanh method to develop a novel Structure. Second, the design uses six NMOS transistors, operates at 2.4 GHz on a 1.8V supply voltage, and was built using the 0.18 m CMOS process at UMC [17]. Below is a breakdown of the parts and how much they're worth:

Table 4.2: Component value for Three input transconductance Stage Mixer

Component	Value
LAll Transistor	0.18 µm
WM-M1,M2,M3,M4	80µm
WM-M5,M6,M7,M8,M9,M10,M11,M12	120µm
LoadResistor-R1,R2,R3	500Ω

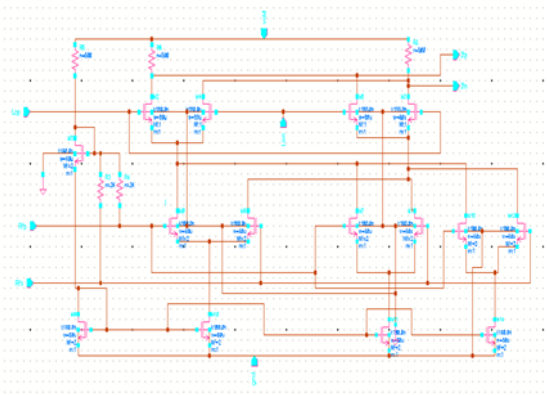

Figure 4.13: Schematic of Double Trans conductance stage Mixer

The bias current for the mixer core and the output buffer stage is controlled by a current mirror via transistors M11 to M14, as illustrated in Figure 4.15. In order to combine the differential RF and LO signals, the V-I conversion is performed using transistors M5 through M10. The frequency conversion is accomplished by switching on and off transistors M1, M2, M3, and M4. For high-frequency work, we've settled on a 500 Resistive load [18].

Test setup for the proposed mixer is shown in Figure 4.16; the Gilbert cell mixer symbol is connected to an extra circuit for analysis purposes. Here, a voltage source (port2) connects directly to the LO port of the Mixer in order to deliver the input LO voltage at a frequency of 2.25GHz.The balun, which supplies the differential input RF signal from a single source (port1), is linked to the mixer's RF port.Port3 is used for monitoring the IF signal at the output. The power source for the mixer is 1.8V.

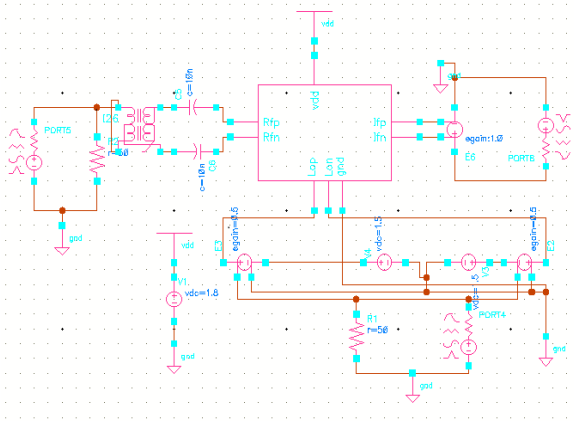

Figure4.14: Test Bench of Double Trans conductance stage Mixer

4.4 Simulated Result of Mixer

In order to model the mixer circuit, the magic simulator is used. The mixer is calibrated for a voltage of 1.8V. The suggested mixer's simulation results are shown in Figures 4.15 through 4.18. Figure 4.15 shows the approximate

12.5dB increase in voltage conversion that was measured (Swept PSS with PAC). Figure 4.18 displays the measured 15.5dB noise figure of the mixer. The mixers have a 50 impedance setup at both the input and the output.
The effectiveness of linearity is evaluated using a two-tone test.The RF inputs of a mixer receive a second signal. Both the first and second input signals have a frequency of 2.401 GHz, with 2.4 GHz being the RF signal frequency. The 1-dB compression point is located at -10dBm, as indicated in figure 5.11, and the plot of the Input-referred IP3 measured to -1dBm may be seen in figure 4.16. The mixer has a low power requirement of around 10.0 mW at 1.8V.

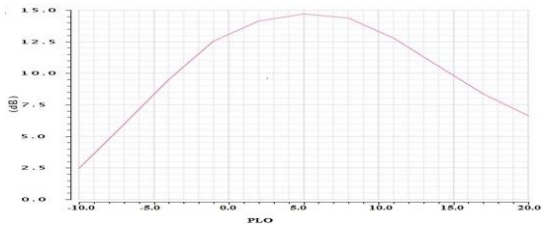

Figure 4.15: Voltage Conversion Gain(Swept PSS with PAC)

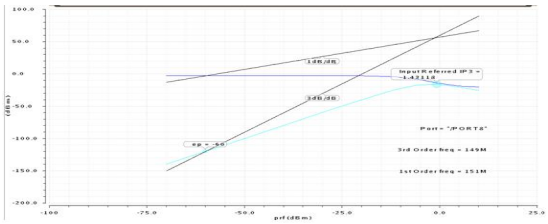
Figure 4.16: Third Order Intercept Point

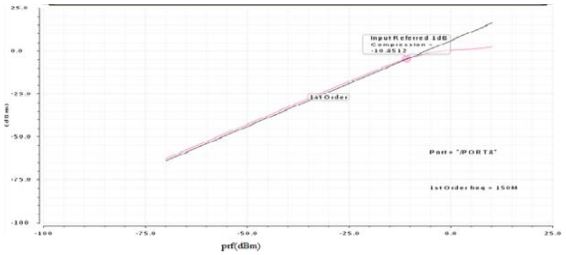

Figure 4.17: 1dB Compression Point

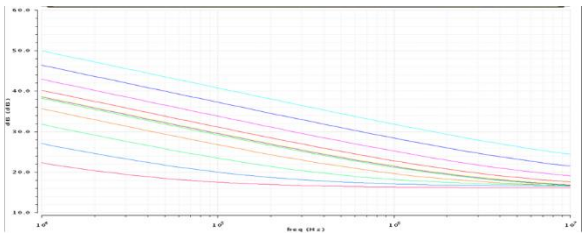
Figure 4.18: Noise Figure

4.5 Layout Design Of Mixer

The planned Gilbert Mixer is shown in Layout form below. The magic editor virtuoso has completed the layout in 180nm CMOS technology. When it comes to a chip's efficient operation, nothing is more crucial than the arrangement of its radio frequency (RF) integrated circuits. Wires used for signal routing have a parasitic effect that reduces IC performance and must be mitigated by careful layout design. While planning the Mixer's layout, we took into account the following elements. Instead of using regular transistors, we switched to the RF kind. Due to its low resistivity and maximum distance from the substrate, Metal-6 has been employed for routing input and output signals because of its low parasitic capacitance.
The schematic for the resistive load Gilbert cell mixer may be seen in Figure 4.19. The design has passed all of our tests.

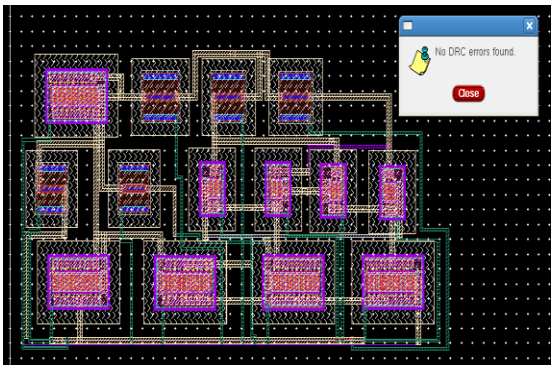

Figure 4.19: Layout view of the Gilbert Mixer

V. Comparison of The Old and New Work

Table 5.1 Comparison of The Existing Work And Proposed Work

S.No.	Parameter	Existing Work	Proposed Work
1	Input RF Frequency	12.5	12.4GHz
2	Input LO Frequency	12.5	2.25GHz
3	Supply Voltage	1.5	1.8V
4	Technology	0.13	180nm
5	Conversion Gain	3db	6.7dB
6	Noise Figure	15.5dB	15.2dB
7	1-Db Compression Point	1.62dBm	-10dBm
8	IIP3	-16.6dBm	-1dBm
9	Power Consumption	45mW	10mW

Table 5.2: Measured result of the two input Transconductance Stage Mixer

S.No	Parameter	Proposed Work
1	Input RF Frequency	12.4 GHz
2	Input LO Frequency	12.25 GHz
3	Supply Voltage	1.8V
4	Technology	180nm
5	Conversion Gain	12.5dB
6	Noise Figure	15.2dB
7	1-Db Compression Point	-10dBm
8	IIP3	-1dBm
9	Power Consumption	20mW

Table 5.3: Measured result of three input Trans conductance Stage Mixer

S.No	Parameter	Proposed Work
1	Input RF Frequency	2.4GHz
2	Input LO Frequency	2.25GHz
3	Supply Voltage	1.8V
4	Technology	180nm
5	Conversion Gain	7.5dB
6	Noise Figure	15.2dB
7	1-Db Compression Point	-10dBm
8	IIP3	-1dBm
9	Power Compression	30mW

VI. CONCLUSION

5.1 Conclusion : Indicative of the work put into creating the Gilbert mixer. It is an illustration of the suggested mixer for doing RF-to-IF down conversion. Because of the better feed through performance and the resultant high linearity, the double balanced cell mixer architecture was adopted in this thesis. In section 5, we show the circuit layout and simulation results for the mixer. The simulation findings reported in section 5 characterized the gain, noise figure, and linearity performance of the converter when fed a 2.4 GHz input signal and a 2.25 GHz signal from the local oscillator. The resulting IF signal had a frequency of 150 MHz. All inputs are valid and within acceptable ranges. The results of the suggested mixers' simulations are listed in Table 5.1.

5.2 Future Work : The RF receiver front-end application is suitable for the mixer that is provided in this thesis. Additionally, input pairs have the potential to attain a greater linearity, but this comes at the expense of an increased power consumption.

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