Design of an enhanced fault tolerant ALU using hardware redundancy technique for low power applications

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***Abstract*— The recent advances in the semiconductor industry have led in the development of more complex components and systems' architectures by allowing fabrication processes to place a higher number of transistors per area of the silicon die .Thus the manufacturing process are less and less reliable. Therefore we need to build systems that will acknowledge the existence of faults and incorporate techniques to tolerate these faults while still delivering an acceptable level of service. In this paper, we design fault tolerant 16-bit Arithmetic and Logical Unit (ALU) circuit using a hard ware redundancy technique namely TMR (Triple Modular Redundancy) technique in which three modules are replicated and given to voter logic. Also we design ALU to achieve less power consumption and highly reliable using Clock Gating. The software used is XilinxISE.**

***IndexTerms*— fault tolerant ALU, Tripler Modular Redundancy, Clock gating, VHDL**

I. INTRODUCTION

As microprocessors became more complex due to technology scaling, they demand fault tolerant techniques capable of recovering the system from a fault with minimum implementation and performance overhead. System reliability is one of major issues in embedded processors schemes as embedded systems covers every branch of science and technology such as communications, automobiles ,military, medical, satellites, consumer etc. The reliability of an embedded system can be defined as its ability to work accurately under the presence of errors. Errors can arise due to multiple sources like power supply variations, coupling, high density charged particles, temporal circuit variations and leakage etc. Due to the radiation from the sun, integrated circuits may damage and produce upsets such as Single Event Upset errors (SEU), Single Event Transient errors (SET) and etc as presented in [1]. These upsets can produce errors in either combinational logic or sequential logic circuits. When a charged particle hits the combinational logic, a SET (Single Event Transient) occurs and resulting in a transient current pulse. A SET becomes SEU (Single Event Upset) if the erroneous value is latched at a memory element. Arithmetic and Logic Unit (ALU) is a major component of any microprocessor. Therefore to design the microprocessor more reliable, there is a necessity for making the ALU unit to be fault tolerant. We approach a fault tolerance mechanism for the Arithmetic and logic unit. A TMR system is composed of three identical devices and voter circuit. The voting logic circuit has the majority voter which takes the majority of inputs to be the output value. So our main concern is to design a highly reliable ALU. Also designing energy efficient devices increases the run time of the devices dependent upon battery and also decreases power consumption of other electronic devices. There are many techniques to reduce power consumption .Clock gating is the mostly used technique to reduce dynamic power consumption without affecting the functionality of the design [11]. In this paper, we use Clock gating mechanism to reduce dynamic power consumption of Arithmetic and Logic Unit.

II. RELATED WORK

A reliable system can de designed by adding redundancy at different levels like module level, gate level, transistor level or software level. In recent years, a lot of research is being done to tolerate errors in combinational and sequential circuits by using redundancy techniques. A TMR (Tripler Modular Redundancy) is a popular and widely used technique of hardware redundancy to cope with transient errors, which triplicates a hardware module and given to majority voter circuit which decides output of the system. El-Maleh and Al-Qahtani proposed a fault tolerance technique for sequential circuits by introducing redundant states for states with having high probability of occurrence in [3]. Mohanram , Touba have proposed a method based on TMR, which based on partial error masking described in [4]. Ahmad T. Sheikh, Aiman H. El-Maleh, Muhammad E. S. Elrabaa, and Sadiq M. Sait proposed a technique based on protecting sensitive transistors in which a subset of transistors necessary are duplicated for giving the protection of transistors due to errors [5]. In designing of fault tolerant microprocessors , power consumption is becoming another major drawback. Power dissipation in circuits is due to static and dynamic power dissipation. Bishwajeet Pandey, Manisha Pattanaik proposed a method to reduce dynamic power consumption in ALU using clock gating [12].

III. FAULT TOLERANT SYSTEM

In today's world reliability have become increasingly important in all embedded system applications. The property of a fault tolerant system is to continue operating the system properly during the presence of failure of components and a backup component or procedure can immediately take its place with no loss of service [6]. Safety critical applications need systems to

operate correctly even in the presence of faults. Fault can be defined as a variation from the expected behavior of the logic. Faults can be classified as transient, intermittent or permanent. Transient fault is a fault that appears for a short period of time and disappears later. The transient faults occur due to design errors and environments. An intermittent fault is one that appears, disappears and reappears. It oscillates between active and quiescent. When the fault is active, the system failures from its operation. When the system is quiescent, the system works normally. Usually these intermittent faults occur due to lose electrical connections. A permanent fault is a fault that appears and persists until it is repaired. Mostly, the fault tolerance techniques based on redundancy. In Fault tolerant systems, there are four types of redundancy techniques.

Hardware redundancy: Hardware redundancy includes additional hardware components in the system for supporting fault tolerance. In hardware redundancy, basically there are three approaches: passive, active and hybrid. Passive redundancy is used for hiding the fault while the active redundancy used for detection and recovery. The passive redundancy method covers and hides faults, instead of detecting them. The advantage of the passive redundancy is that continuous operation is guaranteed. The techniques used for TMR (Triple Module Redundancy) technique and NMR Technique (N-module Redundancy) Technique. The basic idea of Triple Module Redundancy is to use three redundant modules and implement a majority voter to decide the output of the designed system [7].

Software Redundancy: Software redundancy includes additional objects, modules or programs for supporting the fault tolerance [6]. Software redundancy typically uses the following techniques such as single version software techniques, multiple version software techniques, or multiple data representation techniques which resembles hardware techniques.

Information redundancy: Information redundancy is used to tolerate errors in data by introducing the redundancy in data [6]. The techniques used in information redundancy are coding, parity codes, check sum, cyclic codes, arithmetic codes.

Time redundancy: Time redundancy can provide error correction if the computations are repeated more than one time [6]. Time redundancy attempt to reduce the amount of extra hardware at the expense of additional time.

IV. METHODOLOGY

1. Tripler Modular redundancy (TMR)

Tripler modular redundancy is a passive hardware redundancy technique in which three redundant modules are used to compute the same operation in parallel and the correct output is taken from majority voter circuit. Here, we use three ALU modules and if it finds an ALU is faulty out of the three then the two remaining fault free ALUs mask the output of the faulty ALU from the majority voter circuit.

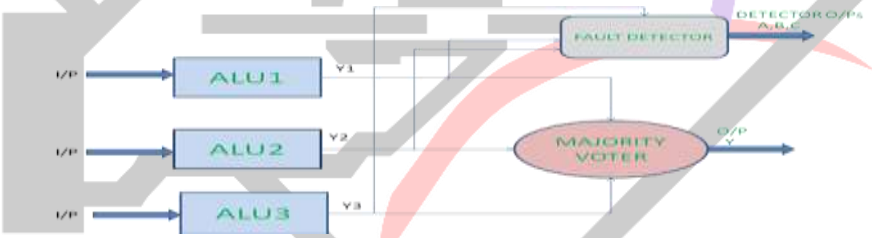

Fig 1 Triple Modular Redundancy (TMR) for ALU

To protect circuits against radiation effects, all registers should be tripled by using this technique. So, this method is also need extra two spare 16 bit ALU and it is give rise to 200% hardware. But this extra hardware is accepted for safety critical applications [8].

A system with N- modular redundancy can tolerate up to 'n' number of module failures, where n = (N-1)/2 [9][10]. Therefore, a TMR (Tripler Modular Redundancy) system can tolerate up to one module failure (n=3-1/2). It is also important to detect which ALU module is failed. A fault detector is used to detect the fault portion of the system. Fault detector has three inputs from output of ALUs and three outputs. The three outputs give which ALU module is faulty. Fault detector is designed by using three XNOR gates. The three outputs are

A= Y1 XNOR Y2;
B= Y2 XNOR Y3;
C= Y1 XNOR Y3;

2. Clock gating

Clock power contributes 50-60% of total power consumption of the circuit. So reducing the clock power is necessary in low power applications. Clock gating is one of the major techniques in reducing clock power. We develop fault tolerant ALU for low power applications is as shown in fig2.

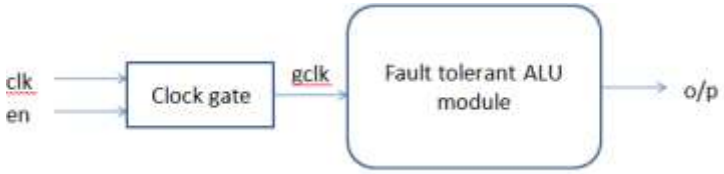

Fig 2 Fault tolerant ALU using Clock gating

V. RESULTS AND DISCUSSION

The simulation results are performed using XLINIX ISE software. The block diagram of fault tolerant ALU as shown in fig 3.It contains three subsystem ALUs, voter logic and a fault detector circuit. The schematic diagram of ALU as shown in fig 4.

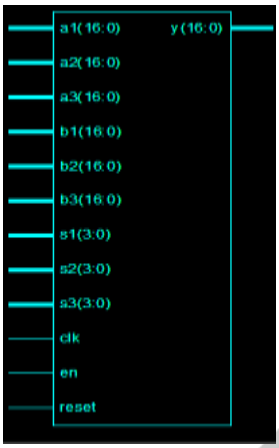

Fig 3:Block diagram

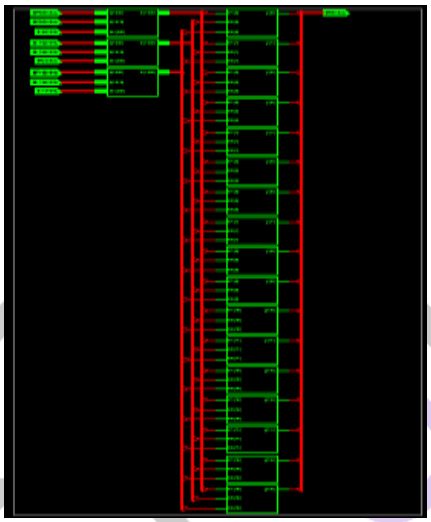

Fig 4:Schematic disgram

The simulation waveform of fault tolearant ALU with TMR and fault detector is as shown in fig5. The fault tolerant module is able to detect and mask the output when ALU is faulty.It also detects which ALU is faulty.

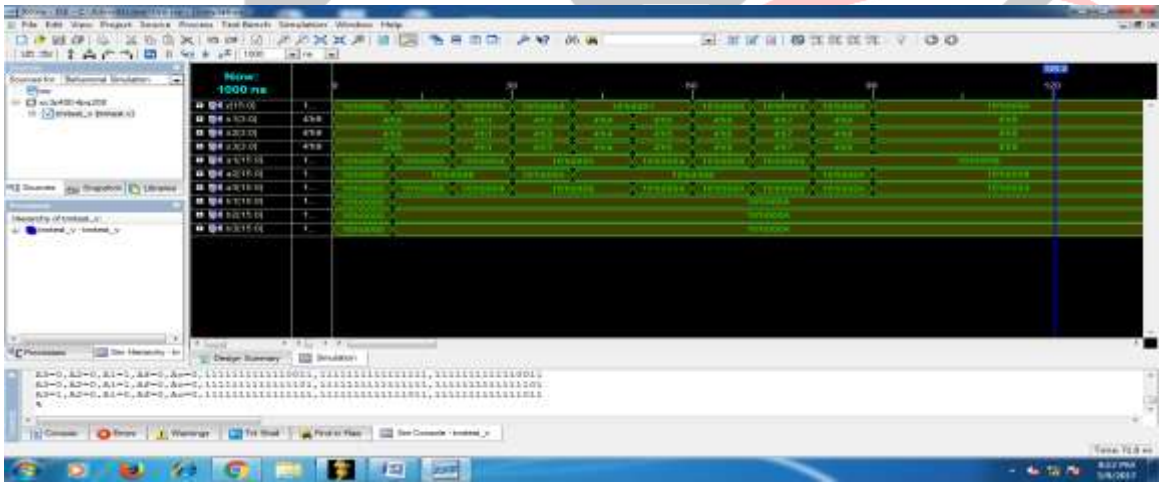

Fig 5:Simulation waveform of fault tolerant ALU

The total power consumption power of the fault tolerant module is estimated using Xpower. The power report is as shown in fig 6 and 7. The area overhead is increased by 200% using the hard ware fault tolerance.But the designed system is more reliable for critical and medical applications.Power overhead is decreased by using clock gating technique.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		45
Peak Power consumption::		43
Vccint 1.20V:	5	6
Vccaux 2.50V:	7	18

Fig 6: power report of fault tolerant ALU without clock gating

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		24
Vccint 1.20V:	5	6
Vccaux 2.50V:	7	18
Vcco25 2.50V:	0	0

Fig 7: power report of fault tolerant ALU with clock gating

Without clock gate	45mw
With clock gate	24mw

Table 1: Comparison of power consumption of fault tolerant ALU

VI. CONCLUSION

The advantage of hard ware redundancy techniques is that continuous operation guaranteed but they present area overhead. The fault tolerant ALU is designed with Tripler Modular Redundancy and fault detector output circuits. Power consumption of the system is estimated through Xpower. The system detects the faulty ALU module from transient faults and mask the output by majority voter logic. Hence, the proposed system is successful in bringing fault recovery and most reliable design and also the power is reduced by almost 50% by using clock gating technique. But the proposed system has also some drawback of area overhead. The proposed system can be used in critical, space and medical applications. In Future, the area overhead of the system is decreased by using hybrid fault tolerance techniques.

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