

Performance Analysis of Different Adiabatic Logic Families

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Abstract— With the increase in demand of portable electronic devices, it is necessary to design circuits with low power dissipation. Adiabatic logic design satisfies this need of low power dissipation by reducing power due to unwanted switching activity. Adiabatic logic state refers to the change of state that occurs without gain or loss of heat. Some of the partial and fully adiabatic logic families are analyzed with 2*1 multiplexer using Tanner EDA tool. All the adiabatic logic families achieve reduction in power dissipation compared with conventional CMOS logic. Among the adiabatic logic circuits, Efficient Charge Recovery Logic (ECRL) design results in 80% of power reduction when compared with conventional CMOS logic. Hence, 4*1 and 8*1 multiplexers are designed with ECRL logic which results in 42% and 39% of power reduction respectively.

Keywords—Adiabatic logic; CMOS Logic; MUX; Tanner EDA tool; Power dissipation

I. INTRODUCTION

Need for low power VLSI chips arise from the evolution of new processing technologies which contains large number of integrated circuits. The Intel microprocessor 4004 developed in 1971 had 2300 transistors, dissipating power of about 1 Watt at 1 MHz frequency. Similarly, the Pentium processor which was developed in 2001 has 42 million transistors, dissipating 65 Watts of power at 2.4 GHz frequency. Due to the fast development in processor industries, a single processor is capable of having billions of transistors within it. Hence, increase in power dissipation of processors would result in dissipation of power similar to that of a nuclear reactor. Such high power density results in low performance because of electro migration, thermal stresses etc. Hence there comes the need for low power dissipated circuits.

Another important need for low power chips is the increased market demand for portable electronic devices powered by batteries. In conventional CMOS devices, power dissipation occurs mainly during switching activities. This power dissipation is reduced by reducing V_{dd} and C_L or by power gating circuits. But adiabatic logic circuit reduces power due to unwanted switching activities. Hence, adiabatic logic circuits gains advantage over CMOS logic. The adiabatic logic circuit uses constant current source instead of constant voltage source as in case of conventional CMOS circuits. The constant current is capable of retrieving the energy back from the circuit and can reuse it.

II. ADIABATIC LOGIC CIRCUITS

A. CMOS Logic Circuits

Power dissipation in conventional CMOS logic circuits [3] is mainly due to switching activities. As shown in fig.1, both the NMOS and PMOS transistors can be modeled by including a resistor in series with an ideal switch. The pull-up (M_p) and pull-down (M_n) resistance are connected to the load capacitance C_L .

When the input voltage V_{in} is at logic 1, the load capacitance is charged to V_{dd} through the pull-up resistance. Hence the energy dissipated from the power supply is $C_L \cdot V_{dd}^2$. If it is assumed that the energy drawn from the power supply is equal to that of the energy supplied to C_L , then the energy stored in C_L becomes,

$$E_{\text{stored}} = 0.5 C_L V_{dd}^2 \quad (1)$$

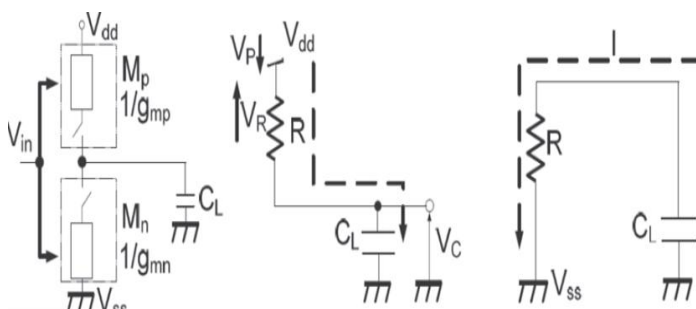


fig. 1 Charging and discharging of CMOS logic

The remaining energy is dissipated in R. Similarly when the input voltage V_{in} is at logic 0, the load capacitance is charged to V_{dd} through the pull-down resistance. Therefore, the total amount of energy dissipated as heat during the charging and discharging of capacitance is,

$$\begin{aligned} E_{total} &= E_{charge} + E_{discharge} \\ &= 0.5C_L V_{dd}^2 + 0.5C_L V_{dd}^2 \\ &= C_L V_{dd}^2 \end{aligned} \quad (2)$$

B. Adiabatic Logic Circuits

Adiabatic switching is used to minimize energy loss during charging and discharging of load capacitance. During adiabatic switching [2], all the nodes are charged or discharged at a constant current in order to minimize energy dissipation. Here the constant current source (time varying voltage source) as shown in fig.2 is used to charge the load capacitance C_L instead of constant voltage source as in case of conventional CMOS circuits.

Thus the energy dissipated using adiabatic switching is,

$$E_{diss} = (RC/T)(1/2CV^2) \quad (3)$$

where T is the charging time. Hence the energy dissipation can be reduced by increasing the charging time.

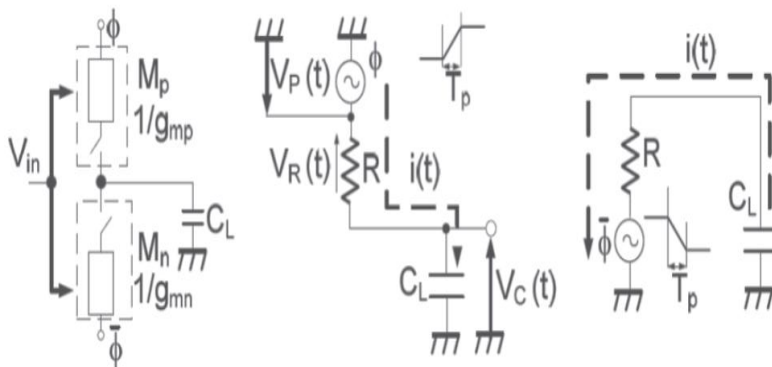


fig. 2 Charging and discharging of Adiabatic logic

C. Power Clock used for Adiabatic Switching

The power clock generator is a major part of the entire adiabatic system design. The power clock generator used here is the combination of power supply and clock (i.e., it consists of frequency and voltage levels). The power clock used in adiabatic systems consists of four phases [11]. Each phase of the clock performs certain operations as shown in fig.3.

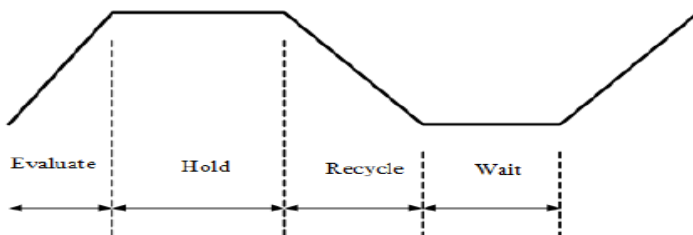


fig. 3 One clock cycle of Power clock

In the evaluation (E) stage, the outputs get evaluated from the stable input signal. During hold (H) stage, the output is kept stable to provide input to the next process. Similarly, recycle (R) stage provides the recovery of power supply and wait (W) stage provides symmetry for next clock cycle to continue.

III. ADIABATIC LOGIC FAMILIES

The adiabatic circuits need “reversible logic” to conserve energy [2]. Adiabatic logic offers a way to reuse the energy stored in the load capacitor instead of discharging the load capacitor to ground. Operations of adiabatic logic circuits are based on the rules such as never turn on a transistor when there is a voltage difference between the source and drain terminals and never change the voltage across the transistor suddenly.

Adiabatic logic families are classified as:

- a) Partial Adiabatic
- b) Fully Adiabatic

A. Partially Adiabatic:

In partial adiabatic some charges gets transferred to the ground in the form of heat dissipation. Hence it recovers a part of the supply voltage. Some of the partially adiabatic logic families are:

1. Efficient Charge Recovery Logic (ECRL)
2. 2N-2N2P Adiabatic Logic
3. Positive Feedback Adiabatic Logic (PFAL)
4. Clocked Adiabatic Logic (CAL)

B. Fully Adiabatic:

In fully adiabatic circuits, all the charges gets recovered and fed back to the supply. Hence it becomes slower and complex [12]. Some of the fully adiabatic logic families are:

1. Pass Transistor Adiabatic Logic (PAL)
2. Two Phase Adiabatic Static CMOS Logic (2PASCL)
3. Split-Rail Charge Recovery Logic (SCRL)

IV. LOGIC DESIGN AND OPERATION

A. Efficient Charge Recovery Logic (ECRL)

The ECRL logic shown in fig.4 uses cross-coupled PMOS transistors. It consists of two cross-coupled transistors M1 and M2 and two N-functional blocks [12].

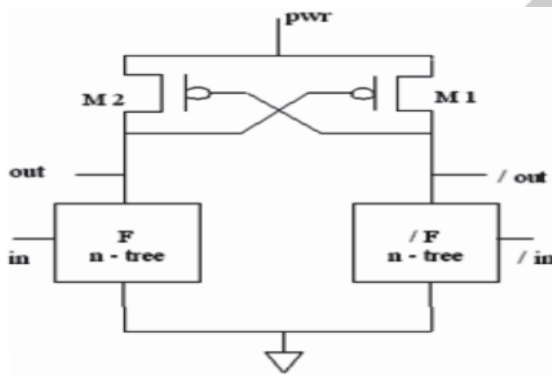


fig. 4 Schematic of ECRL

If the input voltage is high (also the power clock rises from 0 to V_{dd}), output remains at low because input turns on F-tree. When the power clock (pwr) reaches V_{dd}, the outputs hold valid logic levels. After the hold phase, pwr fall down to 0 and output node returns its energy to pwr so that the delivered charge is recovered. These values are used as inputs for the evaluation of the next stage.

B. 2N-2N2P Adiabatic Logic

The fig.5 shows the schematic family of 2N-2N2P family. Its advantage [15] over ECRL is the cross-coupling effect of the NMOSFET switches, which produces non floating outputs during recovery phase. 2N-2N2P logic family differs from ECRL where it has a pair of cross coupled NMOS transistors in addition to the cross coupled PMOS transistors common to both the families.

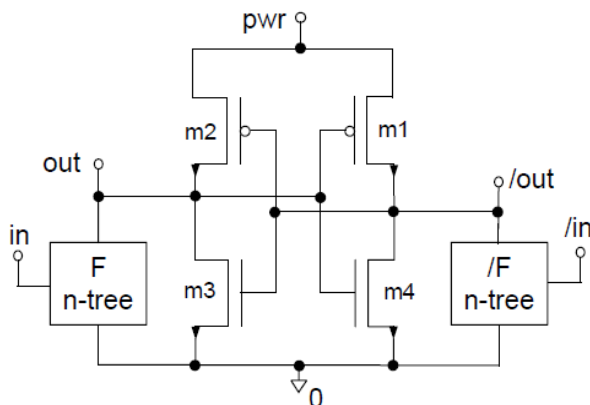


fig. 5 Schematic of 2N-2N2P logic

C. Positive Feedback Adiabatic Logic (PFAL)

PFAL [1] shows the lowest energy consumption when compared with all the other logic families. The schematic of PFAL logic shown in fig.6 consists of two PMOS transistors M1-M2 and two NMOS transistors M3-M4, which avoids logic level degradation on the output nodes.

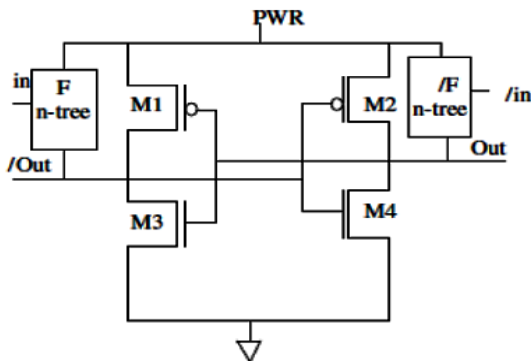


Fig. 6 Schematic of PFAL

This logic family generates both positive and negative outputs. The functional blocks (n trees) are in parallel with the PMOSFET of the adiabatic logic. The two n-trees realize the logic function.

D. Clocked Adiabatic Logic (CAL)

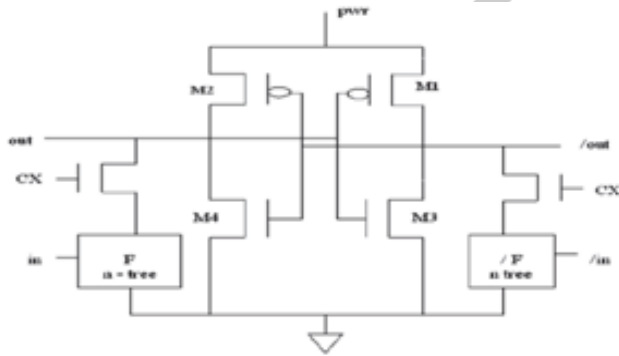


fig. 7 Schematic of CAL

The basic CAL gate [4] is shown in the fig.7. The cross-coupled CMOS inverter formed by transistors M1-M4 becomes the memory unit. The control signal CX controls the transistors that are in series with the logic function n-trees represented in blocks F and /F.

E. Pass Transistor Adiabatic Logic (PAL)

PAL consists of true and complementary transistors NMOS functional blocks (F, /F) and cross coupled PMOS latch (Mp1, Mp2) [4] as shown in fig.8.

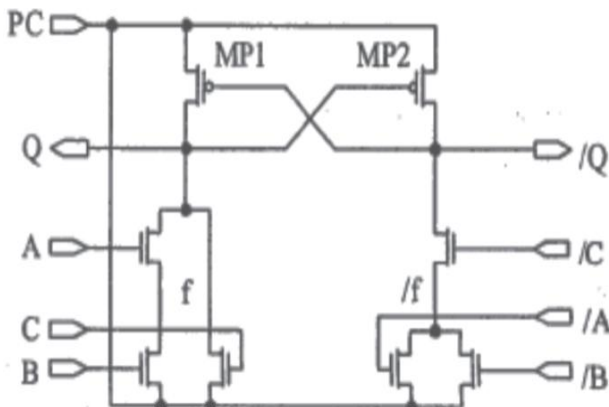


fig. 8 Schematic of PAL

V. IMPLEMENTATION OF MUX

A. CMOS 2:1 MUX

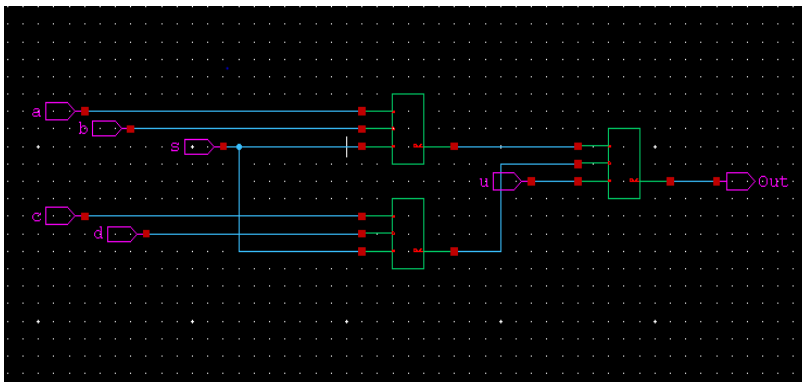


fig. 9 Schematic of 2:1 MUX in CMOS logic

The schematic of the 2:1 mux using CMOS logic is shown in fig 9. As it is a 2:1 mux, it posses 1 select line named s.

B. ECRL 2:1 MUX

The ECRL 2:1 mux schematic is shown in fig 10.

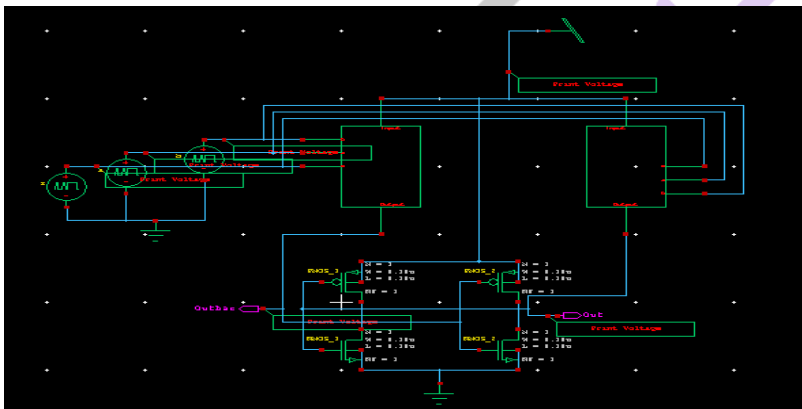


fig. 10 Schematic of ECRL 2:1 MUX

C. ECRL 4:1 MUX

The schematic of the proposed 4:1 mux using ECRL logic is shown in fig 10. As it is a 4:1 mux, it posses 2 select lines named s and u. Here 4:1 mux is designed using 3, 2:1 mux which is also designed using ECRL logic.

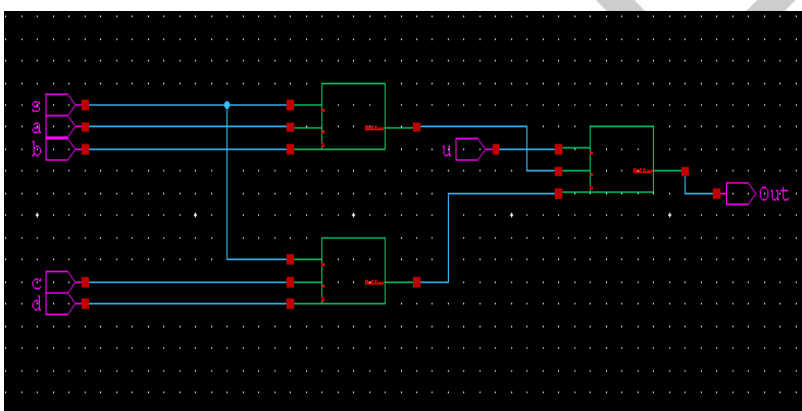


fig. 11 Schematic of proposed 4:1 ECRL MUX

D. ECRL 8:1 MUX

The schematic of the proposed 8:1 mux using ECRL logic is shown in fig 11. As it is a 8:1 mux, it consists of 3 select lines named s , u and v. Here 8:1 mux is designed using 2, 4:1 mux which is also designed using ECRL logic.

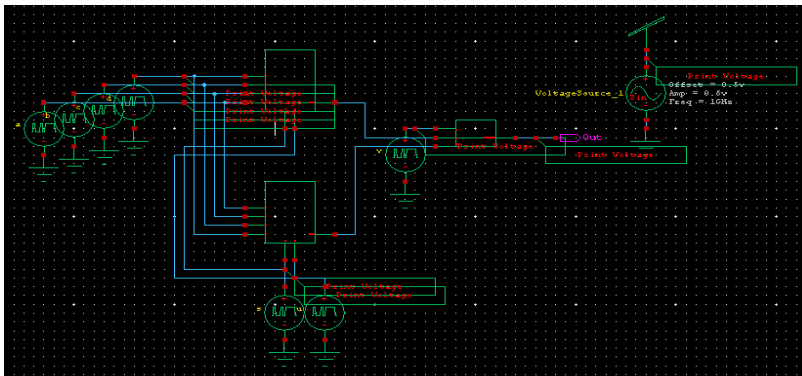


fig. 12 Schematic of proposed 8:1 ECRL MUX

E. CMOS RIPPLE CARRY ADDER

The schematic of 4-bit ripple carry adder is designed using CMOS logic as shown in fig 12.

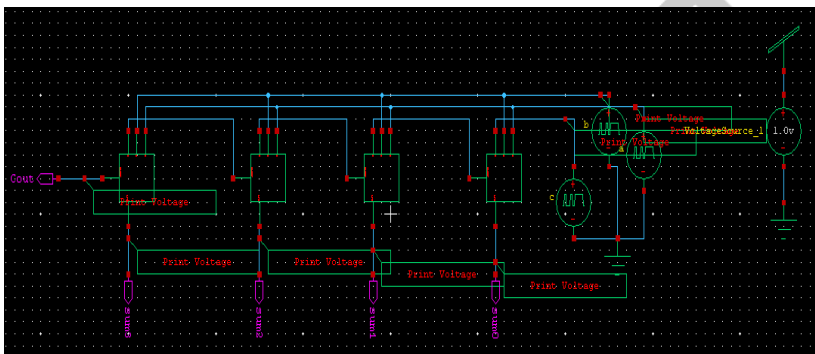


fig. 13 Schematic of 4-bit Ripple Carry Adder

V. SIMULATION RESULTS

A. MUX Comparison

The 2:1 multiplexer (MUX) was designed using CMOS logic in S-Edit of Tanner EDA and simulated in T-spice of Tanner EDA tool. The power dissipation of the circuit is shown in table I.

TABLE I. ANALYSIS OF CMOS 2:1 MUX

Freq (MHz)	Supply volt (V)	Avgpwr (μW) CMOS 2:1 MUX
100	1	2.24
100	1.8	6.78
200	1	2.12
200	1.8	6.42

The 2:1 MUX was designed in all adiabatic logic circuits and simulated in Tanner EDA tool and all logics achieves reduction in power as shown in table II.

TABLE II. ANALYSIS OF 2:1 MUX WITH DIFFERENT ADIABATIC LOGICS

Freq (MHz)	Supply volt (V)	Avgpwr (μW) PFAL	Avgpwr (μW) 2N-2N2P	Avgpwr (μW) ECRL	Avgpwr (μW) CAL
100	1	0.977	1.454	0.297	1.440
100	1.8	2.845	3.988	0.927	4.294
200	1	0.985	1.449	0.286	1.428
200	1.8	2.829	3.952	0.883	4.24

From the analysis of adiabatic logic circuits, ECRL is considered to achieve large power reduction. Hence, 4:1 MUX and 8:1 MUX was proposed using ECRL logic and it achieves large power reduction when compared with conventional CMOS logic as shown in table III and table IV.

TABLE III. ANALYSIS OF PROPOSED 4:1 MUX

Freq (MHz)	Supply volt (V)	Avgpwr (μ W) CMOS 4:1 MUX	Avgpwr (μ W) ECRL 4:1 MUX
100	1	5.076	3.158
100	1.8	15.82	9.13
200	1	4.809	3.184
200	1.8	14.99	9.11

TABLE IV. ANALYSIS OF PROPOSED 8:1 MUX

Freq (MHz)	Supply volt (V)	Avgpwr (μ W) CMOS 8:1 MUX	Avgpwr (μ W) ECRL 8:1 MUX
100	1	12.96	8.534
100	1.8	37.10	22.59
200	1	12.28	8.541
200	1.8	35.15	22.48

A. FULL ADDER

The full adder schematic was designed in CMOS logic using Tanner EDA tool. The results of the simulation were analyzed in table V. From the obtained results of sum and carry, full adder circuit is designed with CMOS logic.

TABLE V. ANALYSIS OF CMOS FULL ADDER

Freq (MHz)	Supply volt (V)	Avgpwr (μ W) CMOS SUM	Avgpwr (μ W) CMOS CARRY
100	1	1.44	1.22
100	1.8	4.56	2.97
200	1	1.37	1.15
200	1.8	4.32	2.63

B. RIPPLE CARRY ADDER

The ripple carry adder schematic was designed in CMOS logic using Tanner EDA tool. The results of the simulation were analyzed in table VI.

TABLE VI. ANALYSIS OF PROPOSED CMOS RIPPLE CARRY ADDER(4 BIT)

Freq (MHz)	Supply volt (V)	Avgpwr (μ W) CMOS RCA
100	1	8.173
100	1.8	33.93
200	1	7.743
200	1.8	32.14

VI. CONCLUSION

In this paper, comparison between different adiabatic logic families and conventional CMOS logic is done using Tanner EDA tool. From the analysis, the adiabatic logic ECRL achieves more power reduction than all other logic design. For the 4*1 mux, ECRL achieves 42.28% reduction in power when compared with conventional CMOS logic. Similarly, for the 8*1 mux, ECRL achieves 39.11% of power reduction when compared with conventional CMOS logic. Hence ECRL adiabatic logic can be used in design of portable low power devices.

REFERENCES

- [1] PreetiBhati and Navaid Z. Rizvi “Adiabatic Logic: An Alternative Approach To Low Power Application Circuits,” International Conference on Electrical, Electronics and Optimization Techniques (ICEEOT), IEEE Journal of pp.4255-4260, March 2016.
- [2] W. C. Athas, L.J. Svensson, J.G. Koller, N. Tzartzanis, and E. Chou, “Low power digital systems based on adiabatic-switching principles, IEEE Trans. VLSI Systems, vol. 2, no. 4, pp. 398-407, Dec. 1994.
- [3] P. Chandrakasan, S. Sheng, and R. W. Brodersen, “Low-power CMOS digital design,” IEEE J. Solid-State Circ., vol. 27, no. 4, pp. 473-484, Apr. 1992.
- [4] G. Dickinson and J. S. Denker, “Adiabatic dynamic logic,” IEEE J. Solid-State Circuits, vol. 30, pp. 311–315, Mar. 1995.
- [5] T. Gabara, “Pulsed Power Supply CMOS,” Technical Digest IEEE Symposium Low Power Electronics, San Diego, pp. 98- 99, Oct. 1994.
- [6] AshmeetKaurBakshi and Manoj Kumar, “ Design of basic gates using ECRL and PFAL,”IEEE 2013.
- [7] Blotti, S. Di Pascoli and R. Saletti: “Simple model for positive feedback adiabatic logic power consumption estimation”. *ElectronicsLetters*, Vol. 36, No. 2, Jan. 2000.
- [8] A.Schlaffer and J. A. Nossek, “Is there a connection between adiabatic switching and reversible computing?”,*Institute for Network Theory and Circuit Design*, Munich University of Technology.
- [9] K. Lo and P. C. H. Chan, “An adiabatic differential logic for low power digital systems,” IEEE Trans. Circuits Syst. II, vol. 46, pp.1245–1250, Sept. 1999.
- [10] V.G. Oklobdzija, D. Maksimovic, L. Fengcheng, “Pass-transistor adiabatic logic using single power-clock supply,” IEEE Trans. Circ. Syst. II, Vol. 44, pp. 842-846, Oct. 1997
- [11] PD Khandekar, S Subbaraman, Manish Patil “Low power Digital Design Using Energy-Recovery Adiabatic Logic” International Journal of Engineering Research and Industrial Applications, Vol1, No.III, pp199- 208 1994, pp. 94-97.
- [12] Subhanshi Agarwal and Manoj Sharma, “Semi Adiabatic ECRL and PFAL Full Adder,” in *CSCP*, 2013.
- [13] N. Zhuang and H.Wu, (1992) “A New Design of the CMOS Full Adder,” IEEE Journal of Solid-state Circuits, Vol. 27, No. 5, pp 840-844. R. K. Navi, Md.Reza Saatchi and O.Daei, (2009) “A High-Speed Hybrid Full Adder,” European Journal of Scientific Research, Vol 26 No.1, pp 29-33.
- [14] S.Kang and Y. Leblebici (2003), *CMOS Digital Integrated Circuits Analysis and Design*, McGraw- Hill.
- [15] J.Rabey, M.Pedram, “Low Power Design Methodologies”, Kluwer Academic Publishers, 5th edition, pp5-7, 2002.