Modelling of LDMOS Transistor

[1]D.SAI.CHAITNAYA, [2]K.JEEVAN REDDY

[1]PG Student, [2]Associate Professor
Electronics and Communications,
Sreenidhi Institute of Science and Technology, Hyderabad, India.

***Abstract*—LDMOS is extensively used in high power applications as it offers better performance and it can be easily manufactured with existing CMOS technology with slight modifications, hence in this paper we present a model of LDMOS transistor which includes the resistive drift region incorporated in the existing MM20 mosfet model and by varying the resistive drift region lengths and gate oxide material changes in the device characteristics are obtained and these values are compared to find the best gate oxide and resistive drift lengths**

***Index Terms*— compact model, drift region, resistive region, High voltage MOSFET.**

I. INTRODUCTION

MOSFETs are extensively used in low operating voltages to reduce the power consumption of the devices, but in high power handling devices like the switches and amplifiers used in RF we cannot use the regular mosfet as distance between the source and drain is less and they cannot sustain these high voltages, so LDMOS is the special mosfet in which the resistive drift region is added to the mosfet to sustain high voltages, also in the lateral double diffusion mosfet the different regions can be optimized to make the device suitable for high voltages operations, also it is easy to manufacture with the existing Bicmos technology as only the gate drift regions are to be modified during the manufacturing process, also these devices offer less on resistance and high breakdown voltages.

Some advantages of LDMOS are:

Higher drain currents then conventional mosfets.

These can combine with other cells easily and provide good thermal stability when compared with bipolar transistors.

II. LATERAL DIFFUSION MOSFET

Lateral diffusion mosfet can be considered as an extension to general mosfet as the distance between the source and drain is extended and the gate control over the oxide is also not extended up to drain, the field oxide region which is under no gate control is the resistive region that is included to general mosfet this part of the device provides the high voltage capability as the effective electric field is spread along this region, thus the LDMOS can be divided into three region i.e. region-1,region-2 and region-3 [1] ,the region-1 is under the control of the source and the gate voltage, whereas the region-2 is under the control of gate voltage and in region-3 the electrons are control of the high electric field as no gate terminal is there in this region, thus this acts as a resistive drift region, thus as shown in **Figure 1,** the device is divided into D1,D` and n-drift regions. The region D1 is under the control of source and gate, region D` is under the control of gate voltage and the n-drift region is under the control of electric field and field oxide, thus an effective model of LDMOS should include all these regions.

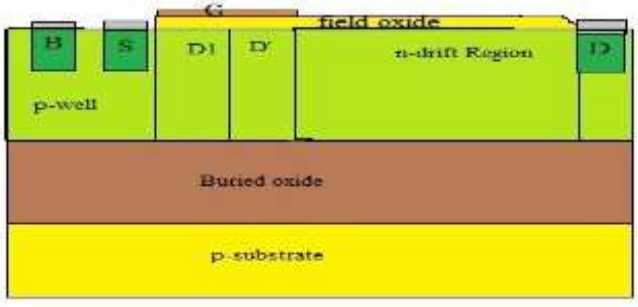

Fig 1. Lateral Diffusion MOSFET

III. DEVICE DESIGN AND SIMULATION

In the process of modeling LDMOS first step is to study the existing MM20 model which is the initial model of mosfet which are operated under high voltages the model proposed in shown below in **Figure 2**.

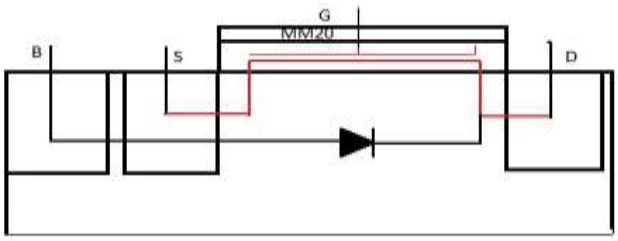

Fig 2 MM20 Model

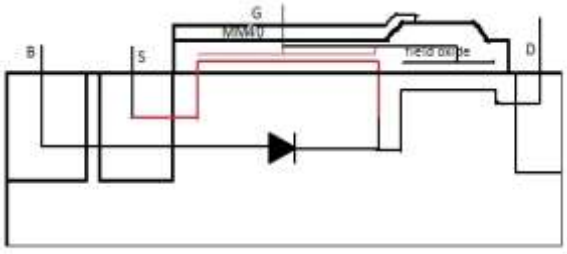

Fig 3 MM40 Model

In the above model there is no drift region so the MM40 model includes the extended gate over the oxide region it is shown in **Figure 3**.Thus adding this region to the existing model the basic ldmos structure can be realized and the equations available with the MM40 model can be used to accordingly to the model that is being developed here [4].

Now with the available tcad tools the proposed model is developed and by using different drift channel lengths, oxide materials the device is simulated. But as the device structure is different from convectional mosfet the charge and the current equations are different, [6] the ward button model charge equations cannot be applied directly because of lateral doping gradient and field dependent mobility. With present charge models present in literature apart from the charges that are assigned to bulk, gate, source, charges are assigned to D1 and D` nodes also. The model for the ldmos is shown as below in **Figure 4.**

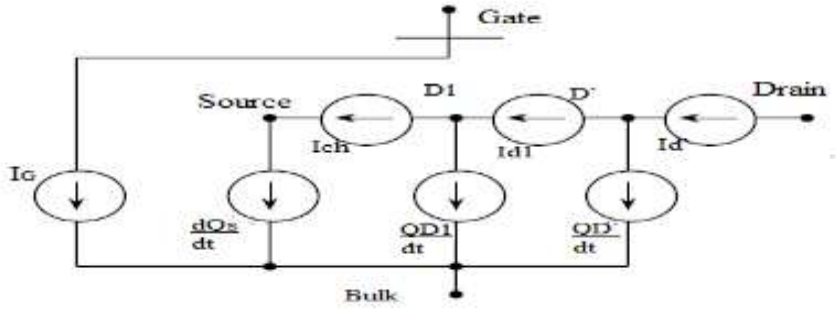

Fig 4. Electrical Model of LDMOS

The device is divided into two regions i.e. one part under the control of gate and the second which is under the control of field oxide. Thus two currents are obtained one is the channel current and the drift current. Channel current is given as

$$Ich = \frac{W\mu_{effch}C_{ox}(Vin0 - 0.5V_{DiSeff})V_{DiSeff}}{L_{ch}\,(1+V_{DiSeff})}$$

Where W is the width of device, μeffch is the mobility of electrons, Lch is the effective channel length, Cox is the gate oxide capacitance and Vin0 =Qinv0/Cox where Qinv0 is the inversion layer charge per unit area at source side. Similarly the current in the drift region is given as

$$Idr = \frac{W\mu_{effch}C_{ox}(Vndr - 0.5V_{D`D})V_{D`D}}{L_{dr}\,(1+V_{D`D})}$$

Here Ldr is the effective drift length, Vndr=Qndr/Cox, it is calculated in the drift region where the charge is calculated depending on the potential between the gate and the drift region, VD`D is the effective potential drop in drift region.

IV.RESULTS AND DISCUSSION

The characteristics of the LDMOSfet are simulated by varying the device parameters. The device parameters used are: channel length, drift length and oxide thickness. The different channel lengths used 1.8um and 2.2um, the different oxides are silicon dioxide, hafnium oxide with width of 100nm and gate width of 100nm.The different concentrations used are for source and drain we have n doping of 1e16 and the drift region is doped with a concentration of 2e16.Now the output of the device are obtained by varying Vds and Vgs voltages keeping one as constant and varying the other parameter respectively.
The drain voltage and gate voltages are varied in the steps of 0,5and 10 volts.

The Vds vs Ids graph are shown below for two gate voltages 5, 10 volts, the dotted curve represents device with silicon dioxide as oxide and dark curve represents hafnium oxide as gate oxide respectively. X-axis represent Vdd drain voltage and Y-axis represent current.

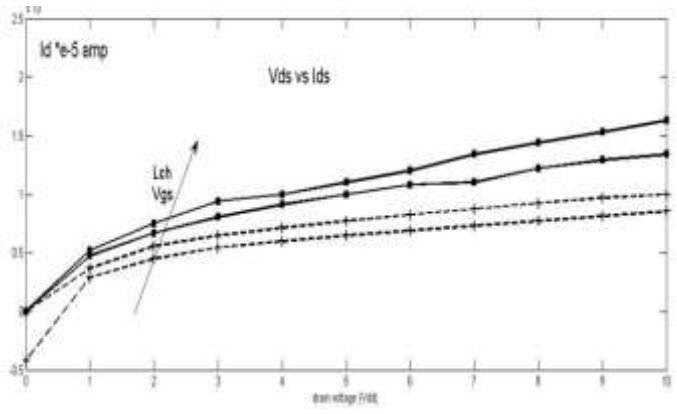

Fig 5: Channel length 1.8um

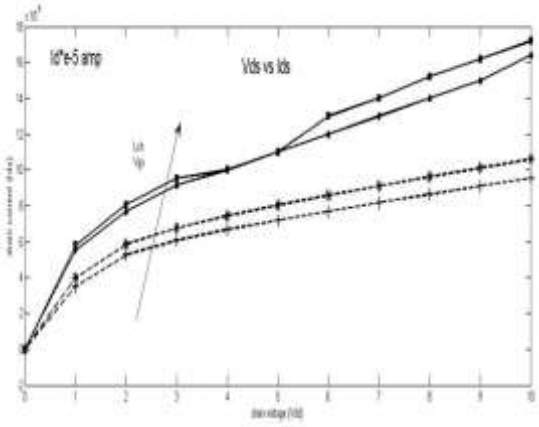

Fig 6: Channel length 2.2um

The Vgs vs Ids graph are shown below, the dotted curve represents device with silicon dioxide as oxide and dark curve represents hafnium oxide as gate oxide respectively. The drain voltages are applied as 0, 5, 10, 15 volts respectively. X-axis represent Vgs gate voltage and Y-axis represent current.

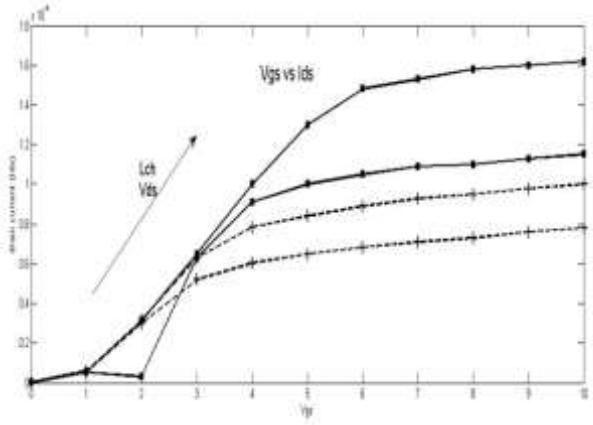

Fig 7: Channel length 1.8 um

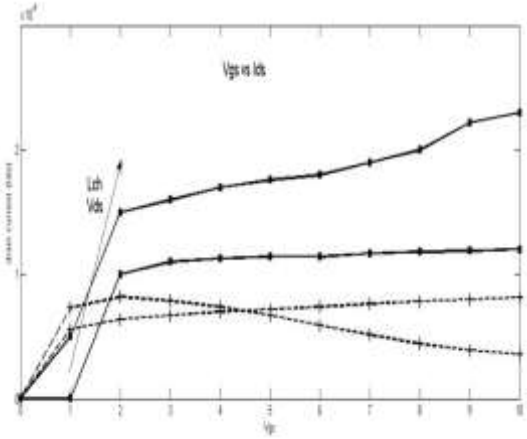

Fig 8: Channel length 2.2um

From the above graph it clearly shows that device with hafnium as oxide has more output current, also by comparing the two graphs one with device drift length as 1.8um and another with drift length as 2.2um the device with higher drift length has more output current.

V. CONCLUSION

Thus model of an LDMOSfet is developed, then models with two channel lengths such as 1.8um and 2.2 um are modeled and different oxide combinations are used in filed oxide and gate oxide to study the characteristics of device, with the available graphs we can observe that device with greater drift length has more output current which suggests that the drift length can be modified according to the output current requirement.

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