DESIGN OF TWO-STAGE CLASS AB CASCODE OP-AMP WITH IMPROVED GAIN

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***Abstract*— Operational amplifier is a main block in analog and mixed-signal-processing circuits, such as D/A, A/D circuits and switched-capacitor circuits and filters. The speed and accuracy of operational amplifier depends on the bandwidth and gain of the op-amp. The main drawback of single stage operational amplifier is low open loop gain. A typical op-amp designed with differential stage, intermediate gain stage, and a class AB stage. In this paper, various two stage class AB op-amps are analyzed. The two-stage class AB cascode op-amp with current replicating branch using an adaptive load is proposed to achieve high gain and symmetrical slew rate. Class AB operation is achieved by the combination of current replicating branch with scaled down transistors and adaptive loads at the output stage. The main advantage of class AB amplifier is symmetrical slew rate and low static power dissipation. This paper shows the analysis like transient response, AC response in Cadence 180nm CMOS Technology.**

***IndexTerms*— op-amp, class AB amplifier, slew rate, gain, CMOS.**

I. INTRODUCTION

Operational amplifier is a main building block in many analog and mixed signal circuits. The various electrical parameters such as gain, phase margin, unity gain bandwidth, slew rate etc all have taken into consideration during designing of op-amp. Better compensation strategy and technique has to be needed to meet the desired specification. In various techniques the two-stage op-amp is used to achieve high gain [5].

The two stage op-amps are used for low voltage applications for which both gain and symmetrical slew rate are of great importance. In some high-speed applications, high slew-rate and fast-settling is required. The slew rate of a two-stage op-amp is depends on bias current. But the drawback of increased bias current is more power dissipation [6]. The slew-rate for a Class-A op-amp is directly related to its static power dissipation. Hence, a higher slew-rate in a class-A op-amp implies higher static power dissipation. In order to maintain less static power dissipation a small additional circuitry Class-AB output stage is used to generate output currents that are essentially larger than the output stage bias current [10]. Adaptive biasing and current replicating branch is another technique to achieve better slew rate without increase in power and cascode amplifier at input stage is used to improve the gain.

II. LITERATURE SURVEY

In single stage op amps, various efficient schemes are used to achieve high symmetrical slew rate. The main drawback of single stage op-amp is low open loop gain [2]. In multi-stage design, the settling time and gain is improved but it leads to decrease in the phase margin and unity gain frequency. In multi stage fully Differential Op-amp switch non-linearities and even order harmonics are cancelled and dynamic range is doubled. But it needs additional circuitry common-mode feedback circuit (CMFB) to maintain the output common-mode level. This CMFB loop disturbs the DC biasing of the intermediate gain stages and it degrades the gain, performance and may cause instability [8].The two stage op-amps are designed using differential op-amp and common source amplifier which improves the gain [5]. The conventional two-stage Miller op-amp has asymmetrical slew rate with high positive slew rate and very less negative slew rate. This less negative slew rate is due to one of the op-amp output transistor acts as a current source. Hence current is unevenly distributed in positive and negative cycles which give asymmetrical slew rate. To improve the symmetry of slew rate, class AB op-amp is used [7]. The slew rate of a two-stage op-amp is determined by the first-stage bias current and frequency-compensation capacitor. The class AB two stage op-amp [Fig.1] with a very small additional hardware is used to avoid this limitation. It includes a diode connected transistor and small capacitor [1][4]. Here output transistor is not a current source. The current flow in output transistor is varied according to AC signal at output of the first stage. M7 transistor enters into a saturation region in positive cycle where the voltage at the gate of M7 is greater than threshold voltage [9]. M7 transistor enters into a cut off region in negative cycle where the voltage at the gate of M7 is less than threshold voltage. Hence M7 is conducts for more than half cycle and less than full cycle. Thus class AB operation is achieved through the M7&M6 transistors. This does not increase power consumption but the main drawback is miller effect with higher frequencies [3]. The class AB two stage op-amp [Fig.2] with current replicating branch and adaptive load is used to avoid miller effect with higher frequencies. The current replicating branch(CRB) formed by transistors M13 and M9 is used to generate the required bias voltage at the gate of output transistor (M7).This transfers current variations in M1-M2 to output transistor M7 and increases the positive output current but it gives limited negative current. In order to improve negative current adaptive load is used. In this

circuit, the adaptive load is used at input stage. But it gives high power consumption and less gain and asymmetrical slew rate. The proposed two-stage class AB cascode op-amp is used to improve the gain and symmetrical slew rate.

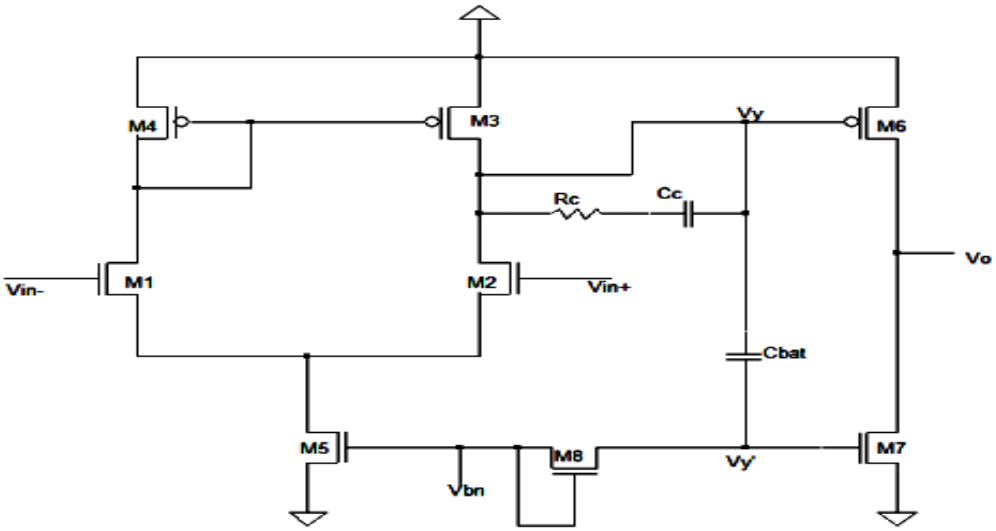

Fig.1 Free-class AB op-amp.

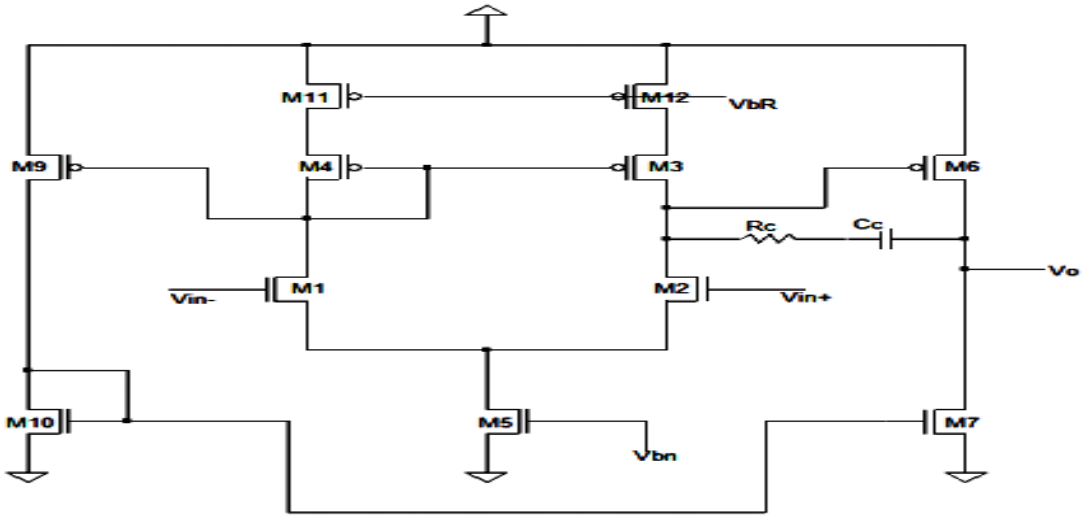

Fig.2 Class AB two-stage op-amp with current replicating branch using an adaptive load

In this paper, the various two stage op-amps are explained in section II. The two-stage class AB cascode op-amp described in section III. The various two-stage class AB op-amp techniques and proposed technique, slew rate, gain and phase plot simulation results are shown and compared in section IV. Finally, section V gives the conclusion and future scope.

III. TWO-STAGE CLASS AB CASCODE OP-AMP

The two-stage class AB cascode op-amp [Fig.3] with current replicating branch using adaptive load is proposed by modifying the existing two-stage class AB op-amp for high gain and symmetrical slew rate operation. It consists of cascode op-amp at input stage and class AB amplifier at output stage. Cascode op-amp at the input stage is used to achieve high gain. The PMOS transistors M3&M4 in cascode op-amp act as a current mirror load. The current mirror loads used for the conversion of differential input to single ended output. It provides higher gain as compared to passive loads. The size of transistors M3&M4 are controlling the maximum of input common mode range, the size of transistor M5 is controlling the minimum of input common mode range. Transistor M6 is contributing the second stage gain. In differential amplifier, the output voltage only varies but current is constant. In order to provide constant current the bias voltage is required. The capacitor (Cc) is used to improve the phase margin and resistor (Rc) is used to reduce the loading effect on capacitor (Cc) and bandwidth. The class AB operation is achieved by current replicating branch and adaptive load. The current replicating branch transfers current variations in cascode amplifier to output transistor M7 and increases positive current. In this circuit, the adaptive load is included directly in current replicating branch to reduce number of transistors. The transistors in adaptive load are operated in triode region due to this resistance increases so output current varies rapidly. Which result is improvement in negative slew rate is approximately equal to positive slew rate.

In this structure, either transconductance of the stage can be improved or the output resistance can be enhanced to achieve high gain. The output resistance is inversely proportional to the bias current while the transconductance is directly proportional to the square root of the bias current. Hence it is power efficient to increase the output resistance by lowering the bias current.

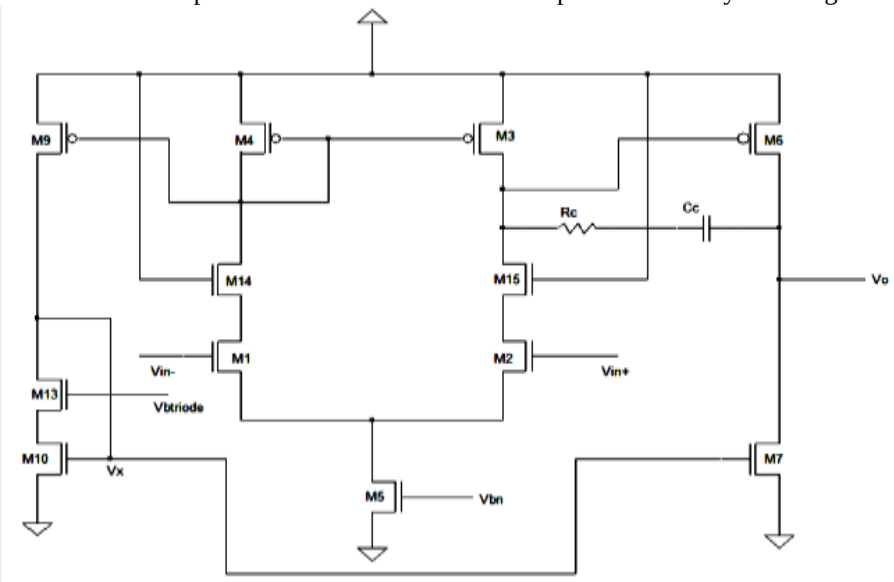

Fig.3 Two-stage class AB cascode op-amp with current replicating branch using an adaptive load.

IV. RESULTS

Slew rate and Gain and Phase Plot have been made with various two stage class AB op-amps and results for free-class AB op-amp are shown in Fig.4 (a) and Fig. 4(b), results for class AB two stage op-amp with CRB using adaptive load at input stage are shown in Fig.5 (a) and Fig.5(b), results for two stage class AB cascode op-amp with CRB using adaptive load are shown in Fig.6(a) and Fig.6(b). The main parameters of two stage op-amps are gain, slew rate, phase margin, gain bandwidth. The slew rate plot gives the positive and negative slew rate. The gain and phase plot gives the gain, phase margin, gain band width. From the Simulation, the gain of the proposed op-amp is 86.63dB is shown in the Fig. 6(a). The proposed op-amp positive slew rate is 17.37v/us and negative slew rate is 18.96v/us with supply voltage 3.3v is shown in Fig. 6(b).

Results for Free-class AB op-amp

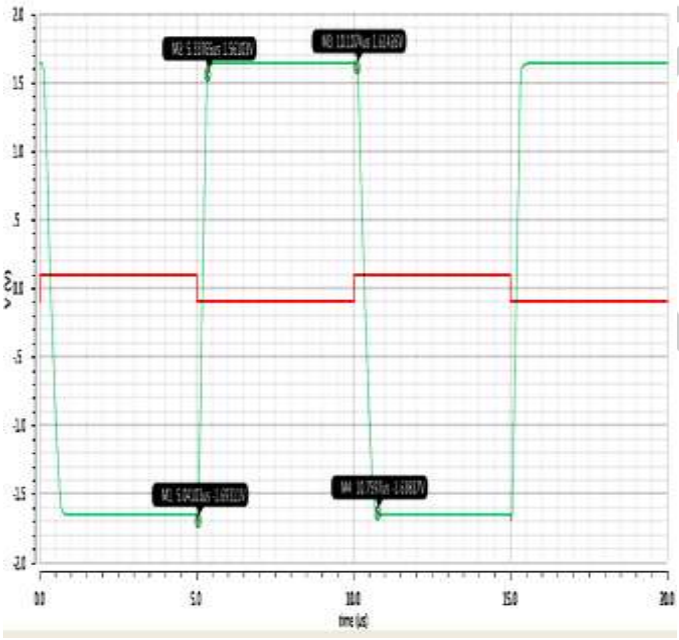

Fig.4 (a) Slew Rate of free class AB op-amp

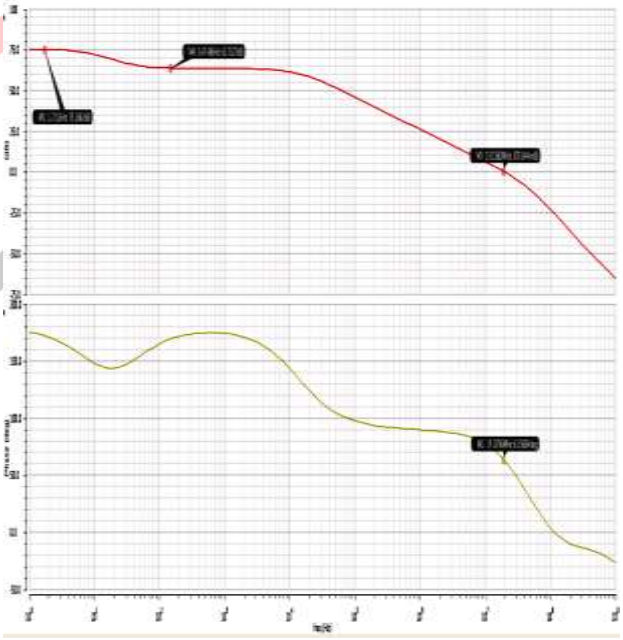

Fig.4 (b) Gain and Phase Plot of free class AB op-amp

Results for class AB two-stage op-amp with current replicating branch using an adaptive load

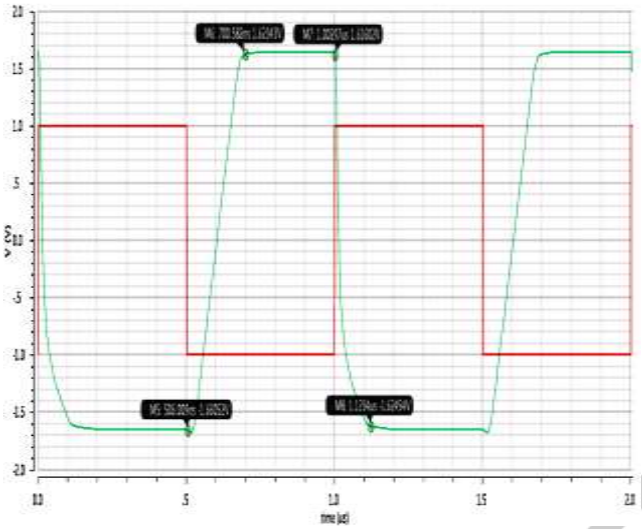

Fig.5 (a) Slew Rate of class AB op-amp with CRB using an adaptive load

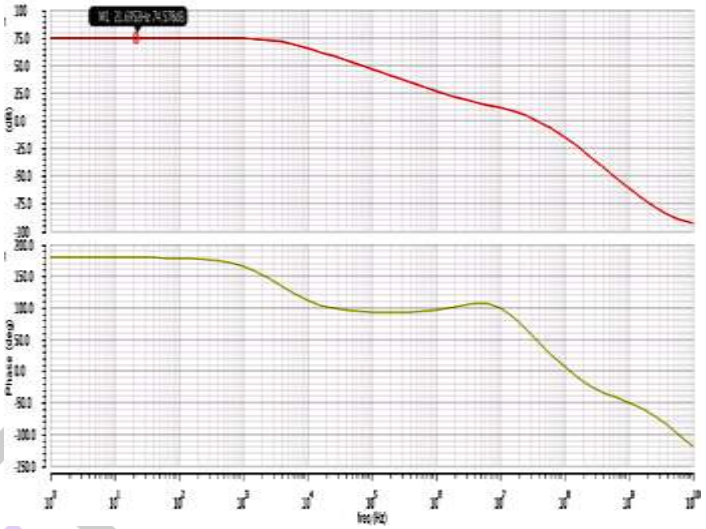

Fig.5 (b) Gain and Phase Plot of class AB op-amp with CRB using an adaptive load

Results for two-stage class AB cascode op-amp with current replicating branch using an adaptive load

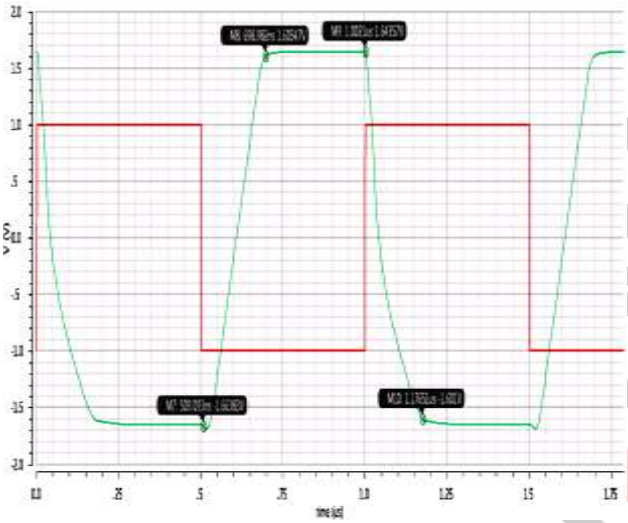

Fig.6 (a) Slew Rate of class AB cascode op-amp with CRB using an adaptive load

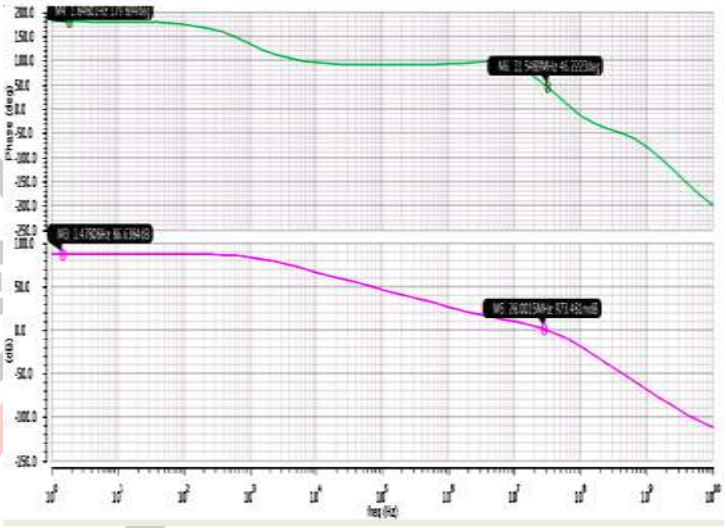

Fig.6 (b) Gain and Phase Plot of class AB cascode op-amp with CRB using an adaptive load

Table 1 summarizes the simulation results of various two stage op-amps. It shows the improvement in gain and symmetrical slew rate of two-stage class AB cascode op-amp as compared to various two stage class AB op-amps.

Table 1.Comparison of various two stage class AB op-amp techniques

Parameter	Free class AB Fig.1	Class AB op-amp with CRB using an adaptive load Fig.2	Class AB cascode op-amp with CRB using an adaptive load Fig.3
Supply (v)	3.3	3.3	3.3
Power(mw)	1.24	1.32	1.31
SR-(v/us)	5.05	27.27	18.96
SR+(v/us)	10.95	16.96	17.37
Ao (dB)	75.18	74.57	86.63
GB (MHz)	19.17	26.30	31.54
PM (^{0})	63.58	50.26	46.22

V.CONCLUSION AND FUTURE SCOPE

The two stage class AB op-amps are presented in 180nm CMOS technology with different analysis. This two stage op-amps require dual supply voltage of 3.3V to improve the gain. The simulation results show that the proposed two stage class AB cascode op-amp is advantageous interms of gain and symmetrical slew rate. The results about Transient response and AC response have been discussed. This two stage op-amp is used for low voltage applications for which both gain and symmetrical slew rate are of great importance. In future, two Stage class AB cascode op-amp can be designed using single miller compensation capacitor (SCMC) with nulling resistor to increase the phase margin, which indirectly makes system more stable..

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