AUDIO PROCESSING DESIGN AND ITS IMPLEMENATION ON ARTIX7 FPGA FOR COCHLEAR IMPLANT

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***ABSTRACT*: Cochlear implant is the device used to restore the hearing capacity for deaf person. This device uses a speech processor in its device which is used for processing the audio signal. The continuous interleaved sampling algorithm is mostly used in the speech processor because it produces the output signals in the non overlapping fashion which reduces the mixing of information between one signal and other. The design in this paper uses a FFT(Fast fourier transform) filter in place FIR(finite impulse response) and IIR(infinite impulse response) filter for processing the speech in frequency domain, it uses frequency separator to separate the serial array of frequencies, it uses encoder which selects the single frequency channel to amplify using amplifier. This design is interfaced on ARTIX7 FPGA board which has the inbuilt microphone which is used to collect sound, this is processed using the design the processed audio is passed at the output.**

***KEYWORDS*: Continuous Interleaved Sampling (CIS), Finite Impulse Response (FIR), Infinite Impulse Response (IIR), Compressed Analog (CA), Field Programmable Gate Array (FPGA), Micro Electro Mechanical Systems (MEMS).**

1) INTRODUCTION

Cochlea is the sound-related sense organ of the human inner ear. This makes an interpretation of outside sound into nerve impulses and sent to the brain framework.

The hair cells in conjunction with the basilar membrane are responsible for translating mechanical information into neural information. If the hair cells are damaged, the auditory system has no way of transforming acoustic pressure waves (sound) to neural impulses and that in turn leads to hearing impairment. If a large number of hair cells or auditory neurons throughout the cochlea are damaged, then the person with such a loss is diagnosed as profoundly deaf. A cochlear implant is therefore based on the idea of bypassing the normal hearing mechanism (outer, middle, and part of the inner ear including the hair cells) and electrically stimulating the remaining auditory neurons directly [2].

2) PROPOSED SYSTEM

Audio processing using the design

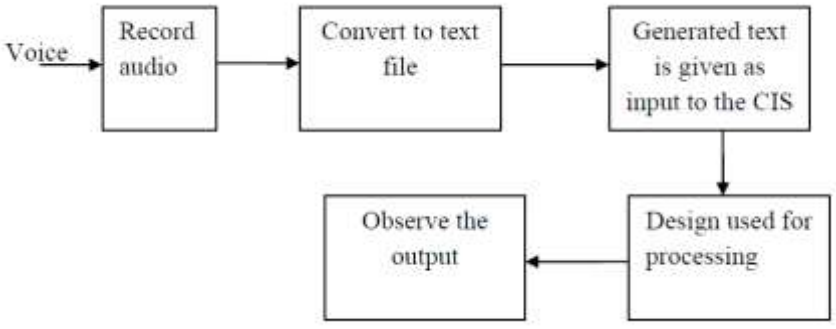

Figure 1: flow of simulation process of audio sample

Figure 1 shows the process of flow in the audio processing. In the simulation process the audio signal is recorded initially in the MATLAB, convert the recorded audio in to a text file generated in hex. The generated hex file is taken as input to the design used for processing which has FFT, frequency separator, encoder, amplifier, and adder. The process is simulated in ModelSim and the output is observed.

The design includes the FFT of the incoming input signal the output of the FFT is connected as input to the frequency separator this is encoded using the encoder and the encoded signal is amplified at the amplifier, the amplified signal is added up at adder. Figure 2 shows the process of design used for processing.

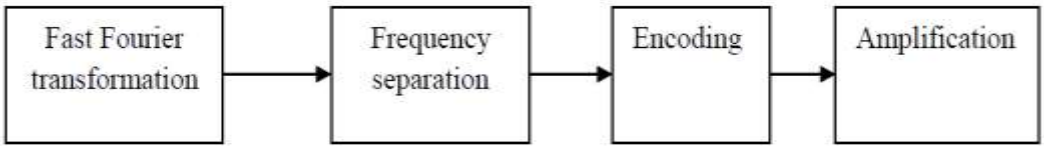

Figure 2: Design used for processing

RTL Schematic of design

The four sub modules of the design are

- FFT
- Frequency separator
- Encoder
- Amplifier

Figure 3 shows the RTL schematic of the processor which has 4 blocks

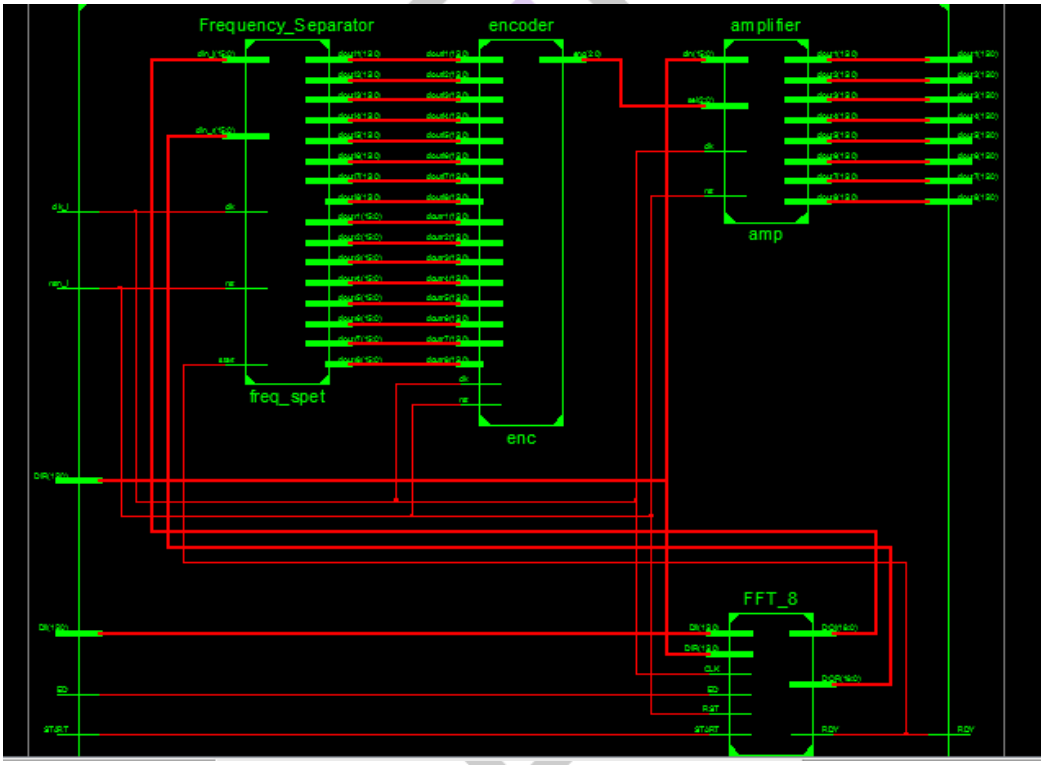

Figure3: RTL schematic of top module

Fast Fourier Transform

The FFT of the input data is done in this process. The 16 bit input data as real and imaginary Data the text created from the recorded audio is taken as real value of the input. In the process of FFT shift the value in the register and perform butterfly operation and the required value is multiplied with the twiddle factor, the data is shifted and taken as a output.
Figure 8 shows the FFT of the value 15 which is 120.

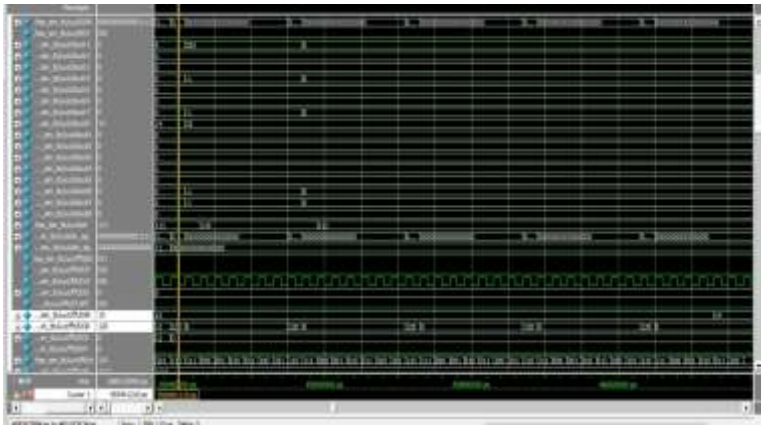

Figure 4: FFT output snapshot

Frequency separator

The frequency separator divides the array of serial data into parallel data at a less clock cycle. In this when the start signal becomes high then the count is done from 0 to 8 when the count reaches the value 8 then the value in the din_r and din_i is produced at the output. In the figure 9 the value 0 and 13 present in the serial array is produced parallel.

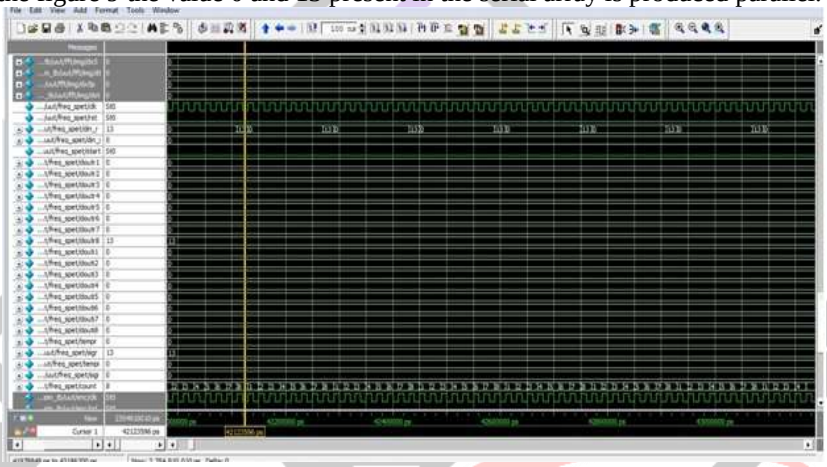

Figure 5: frequency separator snapshot

Encoder

Encoder selects a position of the frequency separator output by using a 3 bit select line. The select line selects the maximum of the input signal present in the input In the figure 6 the value of the encoder is 7 as it has a input value of 13 at position 8.

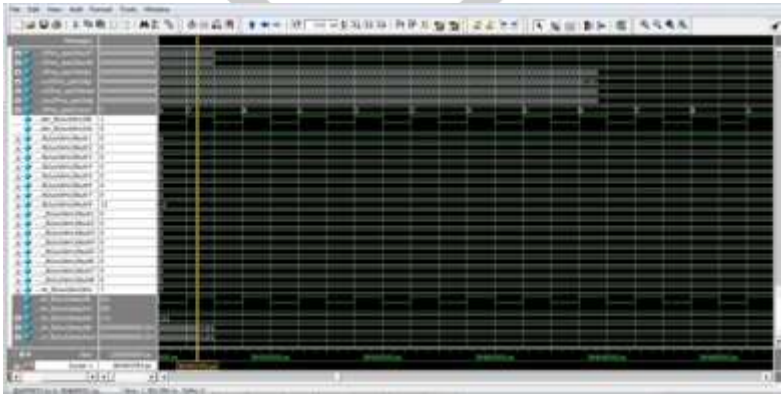

Figure 6: simulation of encoder

Amplifier

The amplifier produces the amplified signal of the encoded data present at the output of the encoder. This produces the output at the non overlapping sequence that is the output of one signal does not overlaps the other. In the figure 7 the select line is at position 5, the input value is 11 and its amplified value is 22 which is shown at position 6 and the other values are zeroes.

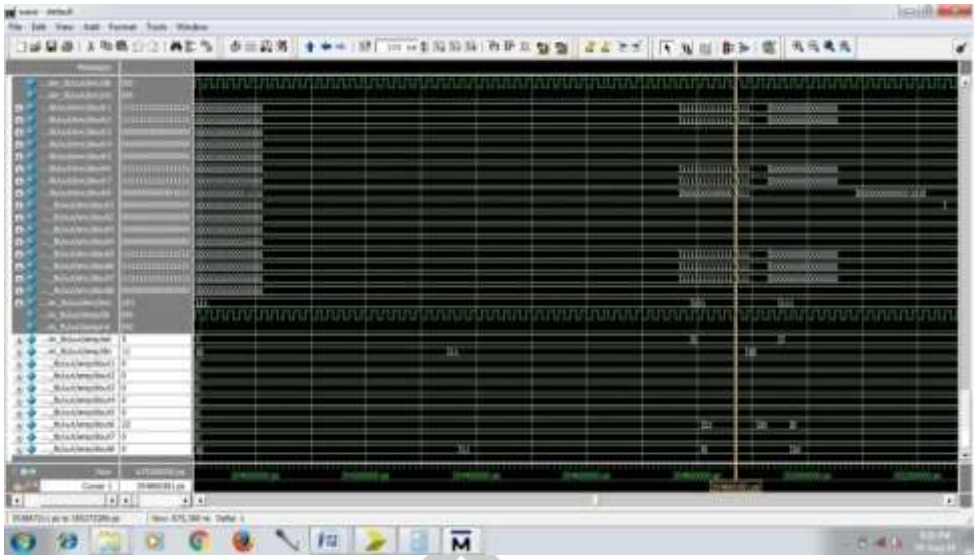

Figure 7: amplifier snapshot

Final output

The amplifier is taken as output, which is the amplified output of the original signal , the eight different outputs are in non overlapping fashion that is one output signal does not co insides other output so that we can send the signal to the electrode in a non overlapping sequence.

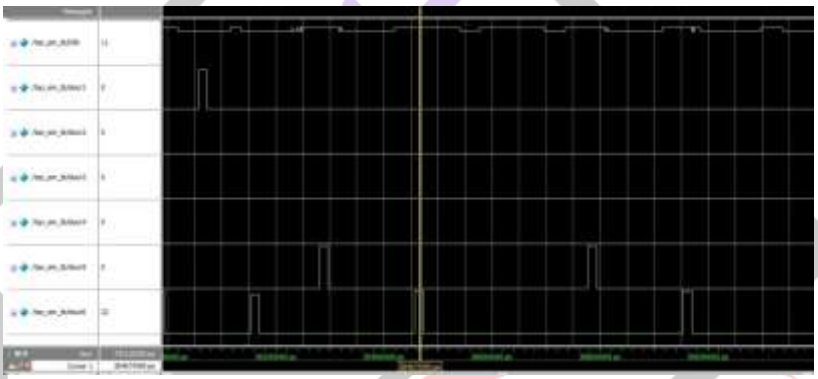

Figure 8: simulation result

Hard ware interfacing with Artix7 FPGA

To test the processed design Artix 7 FPGA (field programmable gate array) board is used for digital circuit development, this FPGA has external memory, Ethernet port, and several other ports are available. The Nexys4 board of Artix 7 FPGA has MEMS microphone which is used to collect sound information from the environment and is converted into electrical energy, this is saved in memory of the board, which is given as input to the design of the processor, the output of the design that is adder output is produced this is given to the audio out demo and to VGA for output, the VGA is connected to the monitor of the computer. Figure 9 shows Hardware design of the project in this the voice signal is taken in real time via microphone of the FPGA this is given to the design used for processing the audio signal the processed output is given to the monitor of the computer via VGA cables and to the output of the audio of the board.

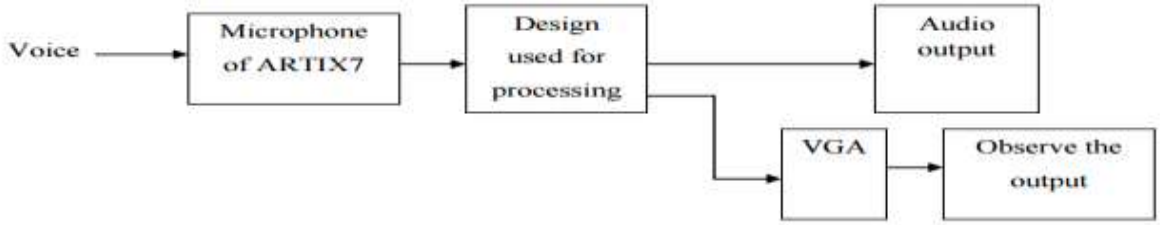

Figure 9: over view of hard ware interfacing

The figure 10 shows interfacing of ARTIX 7 board. The USB cable is connected to take the power from the computer to the ARTIX7 board which is 5v, a 15 pin VGA cable is used to connect the output data to the monitor of the PC.

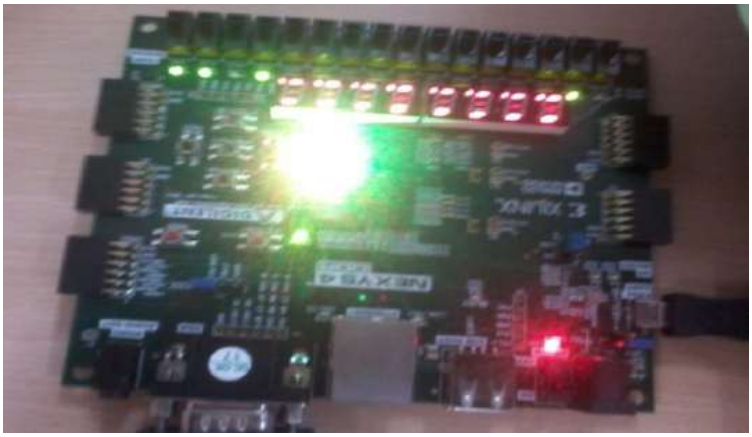

Figure 10: ARTIX 7 board VGA cable connection to the monitor

Figure 11 shows the microphone output in the monitor which is the generated output from the CIS design this is the amplified signal from the design used.

Figure 11: Audio processor with Artix 7 output

3) CONCLUSION AND FUTURE SCOPE

This article represents the implementation of audio processing design using ARTIX7 FPGA board. This board uses nexys4 which is completely usable for digital platform, as it has many inbuilt ports and peripherals it can be used for many application. The proposed design has the advantages of producing the output signal in the non overlapping fashion. This design uses FFT to convert time domain samples to frequency samples the generated data is amplified the amplified signal is added using adder. The adder output is given to the audio output of the FPGA design and to the monitor of the computer. In the future the channels can be increase by using higher point of FFT, the processed audio is used for hearing aid application and for cochlear implant.

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