High Speed 32 Bit MAC using Reversible Vedic Multiplier and Kogge Stone Adder

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***Abstract*—A 32 bit multiply accumulator (MAC) using Vedic multiplier and Kogge stone adder for high speed application is shown in this paper. Multiply accumulators are extensively used in digital signal processing. Speed of MAC depends on multiplier and adder. Vedic multiplier reduces the number of partial products and it is designed using reversible logic gates which assure zero power dissipation. Reversible logic gates are absolutely necessary in the field of quantum computing and it is extremely important in low power applications. Kogge stone adder with an increment logic and carry skip logic are used as 64 bit adder which will considerably reduces the carry propagation delay. The MAC is designed in VHDL and simulation is done in Xilinx 13.2. FPGA implementation is also carried out.**

***Index Terms*— MAC, Vedic Multiplier, Reversible logic, Kogge stone adder.**

I. INTRODUCTION (HEADING 1)

Multiply accumulate operation is one of the basic arithmetic operations widely used in DSP applications.MAC is composed of an adder, multiplier and an accumulator. Vedic multiplier is used for the reduction of partial products and thus by reduces the speed and area. Vedic mathematics is a unique technique of calculations based on 16 sutras (algorithms).Urdhava triyagbhayam sutra is one such algorithm which enables parallel generation of intermediate products and thus eliminates unwanted multiplication steps. Addition is done by using Kogge stone adder. The Kogge stone adder is a parallel prefix adder since the generate and propagate signals are pre-computed.

In a tree based adder carrier is generated in tree and fast computation is obtained at the expense of increased area and power in addition, the delay of 64 bit adder is reduced by using a carry skip logic and incrementation block. Reversible logics are the extremely important in the emerging field of quantum computing and are used to get less power. In the accumulate adder the previous MAC output and the present output will added and it consists of multiplier unit, one adder unit and both will get be combined by an accumulate unit.

II. LITERATURE SURVEY

Multipliers

Due to the regular structure and wiring array multiplier takes up the least amount of area. But the repeated addition and shifting procedure makes it the slowest multiplier. Wallace tree algorithm can be used to reduce the number of sequential adding stages. The irregular structure of Wallace tree makes the layout more difficult. Though booth multiplier will reduce the number of partial products, it will increase the complexity of the circuit to generate partial product bit.

Adders

Slow additions directly affect the total performance of the computer. Ripple carry adder is the simplest and smallest adder design. The carry propagation delay of ripple carry adder makes it as the slowest adder. Carry select adders and carry look adders improves the performance but the design is very complex. Kogge stone adder is the fastest adder. But for the 64 bit adder in the 32 bit MAC, its design is very complex.

III. VEDIC MULTIPLICATION

Urdhva Tiryagbhyam (UT) algorithm is one among the 16 algorithms in Vedic mathematics. The basic idea behind the UT algorithm is that the generation of partial products and concurrent addition of these partial products. By using Vedic multipliers we can eliminate the complex partial product generation step in multipliers. The vertically and crosswise multiplication results in the elimination of shift operation used in partial product generation. Here the partial product calculation is done in single step and thus by we can reduce the power, area and delay of the multiplier. The main advantage of Vedic multiplier is that by using a 2×2 multiplier we can design a 4×4 multiplier.8×8 multiplier can be made from four 4×4 multipliers. Thus any higher order bit multiplier can be made easily by lower order multipliers. A 4×4 multiplier using four 2×2 multiplier is shown in fig.1.The outputs from 2×2 multipliers are added by using ripple carry adders.

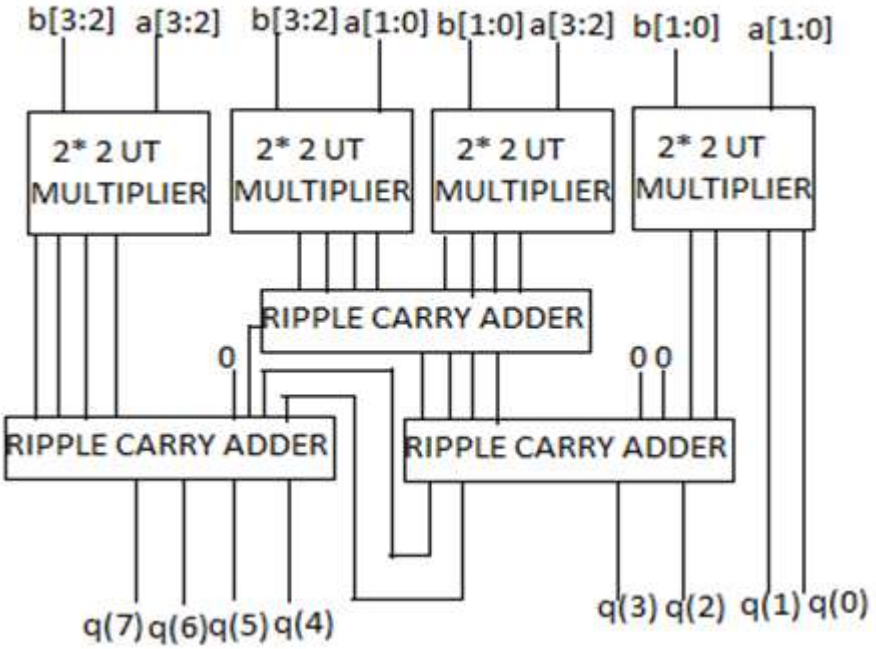

Fig 1:4*4 Vedic multiplier using 2×2 multipliers

IV. PROPSED SYSTEM

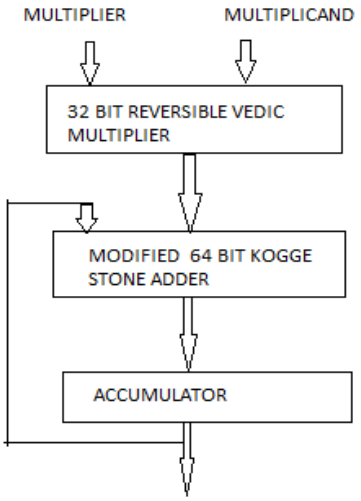

Fig 2: block diagram of proposed MAC

Reversible Vedic multipliers

Conventional UT multiplier can be modified by using reversible logic gates. The power dissipation in a circuit can be reduced by the use of reversible logic. No energy would dissipate from a system if it would be able to return to its initial state from its final state regardless of what occurred in between. In reversible gate, the number of inputs and outputs are equal. So no bit is lost. Hence power dissipation will be reduced. And gate is implemented using Tofoli gate. Reversible half adder is implemented using Peres gate where as full adder is implemented using double Peres gate. Since for any ripple carry adder the input carry for the first full adder is zero, this implicitly means the first adder is a half adder. Conventional half adders and full adders are replaced by Peres gate and double Peres gate.

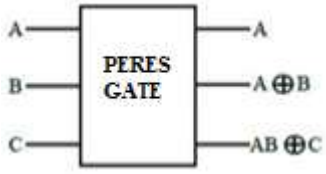

Fig 3:Peres gate

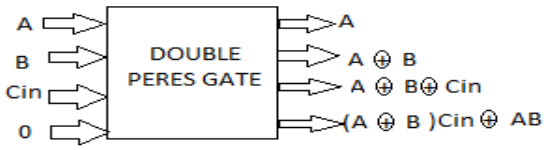

Fig 4:double Peres gate

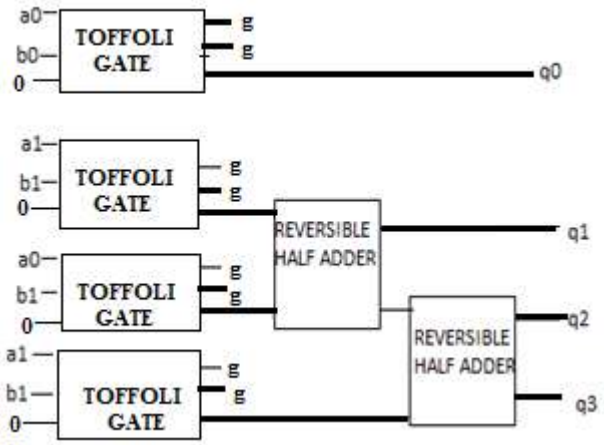

Fig 5:2*2 multiplier using reversible gate

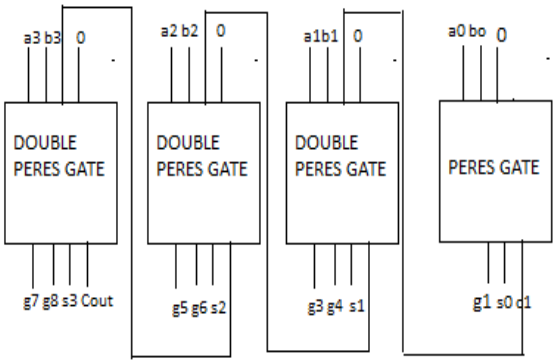

Fig 6:4 bit adder using reversible gates

Modification of 64 bit adder

64 bit adder stage is divided into blocks of 8 bits. Kogge stone adder is used since it is the fastest adder. Addition is done by setting the carry in of each 8 bit adder block to zero. Therefore all the blocks execute their job simultaneously. Then the intermediate output is given to an incrementation block and AOI/OAI block. The incrementation block uses the intermediate results generated by the first stage Kogge stone adder to calculate the final summation. The internal structure of the incrementation blocks which contains a chain of half adders. In order to reduce the delay considerably, for computing the carry output of the incrementation block is not used. The skip logic determines the carry output based on the intermediate results and the carry output of the previous stage as well as the carry output of the corresponding adder stage. The reason for using both AOI and OAI compound gates as the skip logics is the inverting functions of these gates. Thus way the need for an inverter which increases the power and delay can be eliminated. The critical path of the proposed structure contains three parts. These parts include the chain of the 8 bit adders of the first stage, the path of the skip logics and the incrementation block of the last stage.

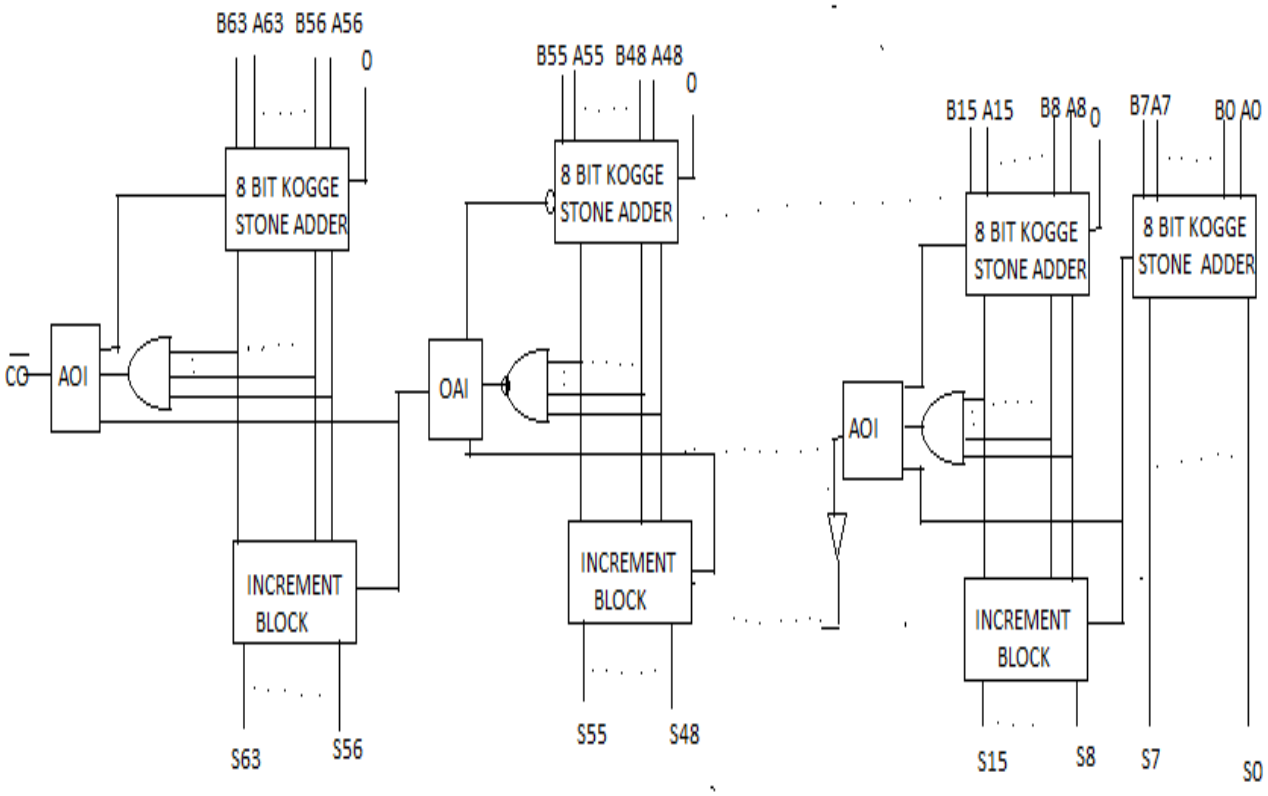

Fig 7: proposed 64 bit adder

Accumulators

Accumulator has an important role in the DSP applications in various ranges and is a very basic and common method. Accumulator is basically a register used to store the intermediate results of arithmetic operations. Here, D flipflop is used as accumulator. Multiplier, adder and an accumulator are forming the essential foundation for the MAC unit. The conventional MAC unit has a multiplier and multiplicand to do the basic multiplication and some parallel adders to add the partial products

generated in the previous step. To get the final multiplication output we add the partial product to these results. Vedic Multiplier has put forward to intensify the action of the MAC Unit [1].

V. IMPLEMENTATION AND RESULTS

The design of proposed MAC is implemented and logically verified using XILINX ISE 13.2 .The delay and area is compared with the existing designs. From the table shown below, it is evident that the delay of the proposed MAC is better than the others.

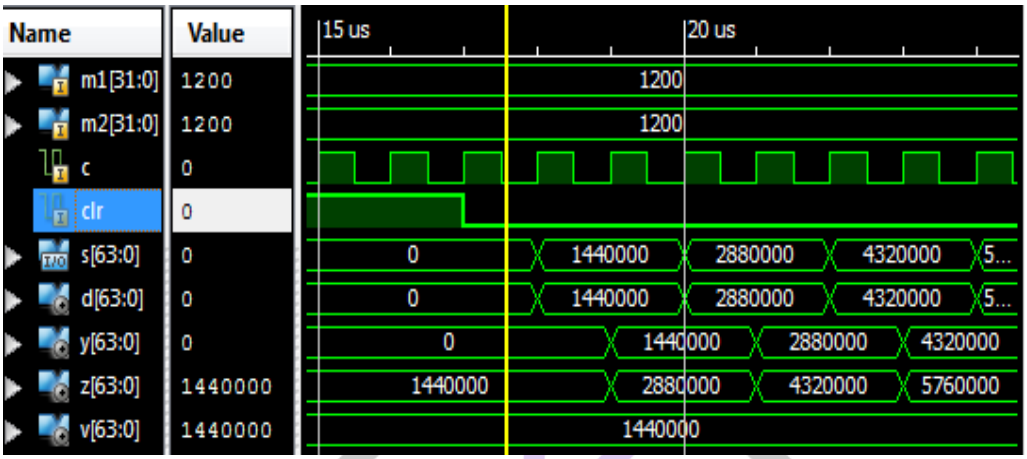

Fig 8: simulation result of proposed MAC

Type of MAC	Delay(ns)	Area(number of slices)	Area –delay product
MAC using booth multiplier and ripple carry adder[2]	108.802 ns	2157	234685.914
MAC using Vedic multiplier and reversible adder[1]	95.247 ns	2239	213258.033
Proposed MAC	79.239 ns	2647	209745.633

Table 1: delay comparison of different MAC architectures

VI. CONCLUSION

Multiply accumulator (MAC) is composed of an adder, multiplier and an accumulator. In the accumulate adder the previous MAC output and the present output will added and it consists of Multiplier unit, one adder unit and both will get be combined by an accumulate unit. Vedic multiplier calculates the partial products in a single step. High performance in terms of area, power and delay can be achieved by using Vedic multipliers. By the introduction of reversible multipliers power can be reduced and the proposed 64 bit Kogge stone adder will considerably reduce the delay at the cost of area and power.

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