Survey of Scan Chain based Low Power Testing

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***Abstract*— In the area of VLSI testing chip failure can occur anywhere, it can be in the flip flops, combinational circuitry or even the Design for testability (DFT) circuitry such as scan chain and logic BIST. Scan chains can be touted as effective aid for logic circuit testing and diagnosis and maximum chip failures occurs due to the defects in the scan chains. This survey is mainly focused on the scan chain defects and scan chain masking for diagnosis of failures in scan based testing.**

***Index Terms*—BIST, Design for testability, scan chain masking, scan based testing.**

I. INTRODUCTION

Time, power and test data volume are among some o the challenging issues for testing the VLSI systems and have not been fully resolved. The power and energy may increase significantly during testing .this extra power consumption may give rise sever hazards to the circuit reliability and effectively increases the test cost and Time. There are several factors which evaluates the power properties of CUT(Circuit under Test).Mainly switching activities generated during the testing of the circuit directly affects on the power consumption and test time .When Flip-Flops are connected in series forms a Scan chain and when two or more scan chains are connected in parallel forms multiple scan chains. Scan chain is a technique which makes the testing of the digital circuits easier by providing simple method to observe each and every flip-flops in the design .In this work diagnosis of multiple failures in multiple scan chains were proposed to reduce the power during testing.

Shrevin sharifi and mohammad Hosseinabadi proposed a method of reducing test power in SoC testing using a Selective Trigger Architecture .The proposed scan cell will work in 3 modes namely :Shift mode, normal mode and Trigger mode .The architecture reduces the switching activities in the CUT. Scanning the data at higher frequency are possible because MUX s are not used in the scanning path. [1]

T. C. Huang and K. J. Lee proposed a token scan cell architecture for low power testing and achieved great power reduction [2]. Parthik GIRARD discussed a low power Testing of VLSI Circuits Problems and Solutions. In the first phase discussed about the problems associated with testing of the VLSI systems externally and in BIST .In the second phase discussed about the techniques used to overcome the problems mentioned along with reduction in power during testing. [3]

Y.Bonhomme and P.Girard propose a method of reducing the test power during the Testing of SOCs. In this approach including logic power and scan power, a method of reducing clock power by considering an concept called as gated clock scheme for the scan path and clock tree feeding the scan path was introduced. The Idea behind the technique is to reduce the clock rate on the scan cell during each shift operations without adding the test time .The architecture consists of a clock, its speed is half of the speed of the normal speed to activate one half of the scan cells in the path during one clock cycle of the scan operation and the second half of the scan cells in the scan path activated by another clock with speed is equal to hail of the normal speed. The Two clocks are synchronous with system clock and have same but shifted in time period during scan operation. The use of these modified clock operation reduces the transition density in the CUT [4].The results shown that only up to 29% of peak power reduction achieved.

Seongmoon Wang and Sandeep K Gupta proposed an ATPG (Automatic test pattern generator) Technique to reduce the switching activity during full scan testing of sequential circuits. This method of testing exploits all don't cares during scan shifting, test application and response capture to minimize the switching activity in the CUT. Don't cares at primary inputs are used to block the gates which make unnecessary transitions during scan shifting and don't cares at state inputs are assigned with binary values to reduces the transition count. It shown that the length of the test sequence can be reduced by two ways. [5]

- Arranging the scan chains such a way that compatible state inputs are placed in neighboring positions.
- Using more sophisticated K-L Bi partitioning algorithm which assigns don't cares as state inputs.

Mehrdad Nourani and Mohammad Tehranipoor presented a Low Transition Test pattern generator for BIST based Testing. A low transition test pattern generator also called as LT-LFSR(low transition linear shift register) has been implemented which can

be used in scan based combinational and sequential circuits which can be tested .The technique manages the reduction in the average and peak power during testing of circuits by reducing the transitions among the patterns in two dimensions . 1) The vertical dimension between consecutive test patterns (Hamming Distance) and 2) the horizontal dimension between the adjacent bits of a pattern sent to a scan chain. The conventional LFSR can be modified in such a way that it automatically inserts intermediate patterns between its original patterns. [6]

Lung –Jen Lee and Wang-Dauh Tseng Adopted a method a Dual-LFSR reseeding technique for low power testing. The work mainly focused on BIST-based compression method for minimizing the test data volume and hence the reduction in test power. An Dual-LFSR are used as de-compressor to jointly generate the test pattern for a given test set [7]. Umesh Parashar worked by combining test-per-clock and test-per-scan test schemes, using two functional cycle lengths during scan and LT-RTPG(low transition random test pattern generator) as TPG (test pattern generator) achieved an reduction in the switching activity as compared to conventional LFSR –BIST.[8]. Lung-Jen Lee and Chia-Cheng He discussed about a deterministic ATPG for low capture power testing, in this work scan chain clustering method is used and whole architecture works in two modes of operation namely shift mode and capture mode. Scan chain clustering aims at disabling some non-critical scan cells during capture mode without affecting the fault coverage. [9]

Abdallatif S.Abu-Issa and Iyad K.Tumar presented the use of SR-Counter (Switch-tail-ring counter) as low transition TPG in Test-per-clock and Test-per-per-scan BIST Applications. In SR-TPG for test-per-clock BIST TPG was implemented by dividing a register into number of switch-tail ring counters during test mode. The first ring counter will be triggered directly by the system clock and the second one will be triggered using the system clock and control logic of the previous counter and so on for the remaining counters. In SR-TPG for test-per-scan BIST TPG an output of a cell of the TPG will be used to scan-in the test vectors into the CUT inputs and memory elements [10]. A Kavitha and G.Seetharaman designed an low power Test pattern generator (LP-TPG) to reduce the switching activity between the test patterns by combining a LP-TPG ,an m-bit counter ,gray code converter and NOR gate structure and XOR array[11].

II. Conclusion

Several aspects of scan chain based VLSI testing still require improvements:

- External and BIST based testing for low power has requires area minimization
- Multiple faults per chain is important for diagnosing chain failures caused by systematic defects.
- A reliable common solution for test-per-clock and Test-per-scan BIST testing is needed.
- A reliable solution for minimizing the switching activity between the scan cells in a scan chain and test vectors in a test pattern is required.
- A low power solution for diagnosing the multiple faults in a multiple chain failure is needed.

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